Michael T Niemier

List of Publications by Year
in descending order

106	2,798	393982	233125
papers	citations	19 h-index	45 g-index

108	108	108	1984
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Scaling for edge inference of deep neural networks. Nature Electronics, 2018, 1, 216-222.	13.1	299
2	Ferroelectric ternary content-addressable memory for one-shot learning. Nature Electronics, 2019, 2, 521-529.	13.1	217
3	Problems in designing with QCAs: Layout = Timing. International Journal of Circuit Theory and Applications, 2001, 29, 49-62.	1.3	184
4	Nanomagnet logic: progress toward system-level integration. Journal of Physics Condensed Matter, 2011, 23, 493202.	0.7	144
5	On-Chip Clocking for Nanomagnet Logic Devices. IEEE Nanotechnology Magazine, 2010, 9, 348-351.	1.1	131
6	A ferroelectric field effect transistor based synaptic weight cell. Journal Physics D: Applied Physics, 2018, 51, 434001.	1.3	113
7	Analog Circuit Design Using Tunnel-FETs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 39-48.	3.5	99
8	Ferroelectric FETs-Based Nonvolatile Logic-in-Memory Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 159-172.	2.1	75
9	FeCAM: A Universal Compact Digital and Analog Content Addressable Memory Using Ferroelectric. IEEE Transactions on Electron Devices, 2020, 67, 2785-2792.	1.6	75
10	An Ultra-Dense 2FeFET TCAM Design Based on a Multi-Domain FeFET Model. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 1577-1581.	2.2	74
11	Computing in memory with FeFETs. , 2018, , .		62
12	Fabricatable Interconnect and Molecular QCA Circuits. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1978-1991.	1.9	52
13	Design and benchmarking of ferroelectric FET based TCAM. , 2017, , .		52
14	Experimental Realization of a Nanomagnet Full Adder Using Slanted-Edge Magnets. IEEE Transactions on Magnetics, 2013, 49, 4452-4455.	1.2	51
15	Design and Analysis of an Ultra-Dense, Low-Leakage, and Fast FeFET-Based Random Access Memory Array. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 103-112.	1.1	50
16	Experimental Demonstration of Fanout for Nanomagnetic Logic. IEEE Nanotechnology Magazine, 2010, 9, 668-670.	1.1	48
17	Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits. , 2016, , .		48
18	Computing with ferroelectric FETs: Devices, models, systems, and applications. , 2018, , .		48

#	Article	IF	Citations
19	Leveraging Emerging Technology for Hardware Security - Case Study on Silicon Nanowire FETs and Graphene SymFETs. , 2014, , .		47
20	SearcHD: A Memory-Centric Hyperdimensional Computing With Stochastic Training. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2020, 39, 2422-2433.	1.9	43
21	Design and optimization of FeFET-based crossbars for binary convolution neural networks. , 2018, , .		39
22	Quantum-Dot Cellular Automata (QCA) circuit partitioning. , 2004, , .		36
23	Systolic Pattern Matching Hardware With Out-of-Plane Nanomagnet Logic Devices. IEEE Nanotechnology Magazine, 2013, 12, 399-407.	1.1	31
24	Magneticâ€“Electrical Interface for Nanomagnet Logic. IEEE Nanotechnology Magazine, 2011, 10, 757-763.	1.1	27
25	Ferroelectric FET Based In-Memory Computing for Few-Shot Learning. , 2019, , .		27
26	In-Memory Nearest Neighbor Search with FeFET Multi-Bit Content-Addressable Memories. , 2021, , .		26
27	PLAs in Quantum-Dot Cellular Automata. IEEE Nanotechnology Magazine, 2008, 7, 376-386.	1.1	23
28	TFET-based cellular neural network architectures. , 2013, , .		23
29	Power and Area Efficient FPGA Building Blocks Based on Ferroelectric FETs. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 1780-1793.	3.5	21
30	Compact Single-Phase-Search Multistate Content-Addressable Memory Design Using One FeFET/Cell. IEEE Transactions on Electron Devices, 2021, 68, 109-117.	1.6	20
31	Design and comparison of NML systolic architectures. , 2010, , .		19
32	Better computing with magnets - The simple bar magnet, shrunk down to the nanoscale, could be a powerful logic device. IEEE Spectrum, 2015, 52, 44-60.	0.5	19
33	Design of Hardware-Friendly Memory Enhanced Neural Networks. , 2019, , .		19
34	Computing-in-Memory for Performance and Energy-Efficient Homomorphic Encryption. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2300-2313.	2.1	19
35	Seed-and-vote based in-memory accelerator for DNA read mapping. , 2020, , .		19
36	Nontraditional Computation Using Beyond-CMOS Tunneling Devices. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2014, 4, 438-449.	2.7	17

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37	A Computing-in-Memory Engine for Searching on Homomorphically Encrypted Data. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 123-131.	1.1	17
38	MIMHD: Accurate and Efficient Hyperdimensional Inference Using Multi-Bit In-Memory Computing. , 2021, , .		17
39	In-Memory Computing with Associative Memories: A Cross-Layer Perspective. , 2021, , .		17
40	Cellular neural network friendly convolutional neural networks â€" CNNs with CNNs. , 2017, , .		16
41	A Mixed Signal Architecture for Convolutional Neural Networks. ACM Journal on Emerging Technologies in Computing Systems, 2019, 15, 1-26.	1.8	16
42	FeFET Multi-Bit Content-Addressable Memories for In-Memory Nearest Neighbor Search. IEEE Transactions on Computers, 2022, 71, 2565-2576.	2.4	16
43	Clocking scheme for nanomagnet QCA. , 2007, , .		15
44	Fabrication Variations and Defect Tolerance for Nanomagnet-Based QCA. , 2008, , .		15
45	Non-volatile and reprogrammable MQCA-based majority gates. , 2009, , .		15
46	Magnetic Properties of Enhanced Permeability Dielectrics for Nanomagnetic Logic Circuits. IEEE Transactions on Magnetics, 2012, 48, 3292-3295.	1.2	15
47	Advanced spintronic memory and logic for non-volatile processors. , 2017, , .		15
48	Direct Measurement of Magnetic Coupling Between Nanomagnets for Nanomagnetic Logic Applications. IEEE Transactions on Magnetics, 2012, 48, 4402-4405.	1.2	13
49	Switching Behavior of Sharply Pointed Nanomagnets for Logic Applications. IEEE Transactions on Magnetics, 2013, 49, 3549-3552.	1.2	13
50	The Impact of Ferroelectric FETs on Digital and Analog Circuits and Architectures. IEEE Design and Test, 2020, 37, 79-99.	1.1	13
51	System-level energy and performance projections for nanomagnet-based logic. , 2009, , .		12
52	Nonvolatile Lookup Table Design Based on Ferroelectric Field-Effect Transistors. , 2018, , .		12
53	Fault Models and Yield Analysis for QCA-Based PLAs. , 2007, , .		11
54	Threshold Gate-Based Circuits From Nanomagnetic Logic. IEEE Nanotechnology Magazine, 2014, 13, 990-996.	1.1	11

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55	Modeling and Benchmarking Computing-in-Memory for Design Space Exploration. , 2020, , .		11
56	A Novel TIGFET-based DFF Design for Improved Resilience to Power Side-Channel Attacks. , 2020, , .		11
57	Bridging the gap between nanomagnetic devices and circuits. , 2008, , .		10
58	Controlling Magnetic Circuits: How Clock Structure Implementation will Impact Logical Correctness and Power. , 2009, , .		9
59	Exploring the Design of the Magneticâ€“Electrical Interface for Nanomagnet Logic. IEEE Nanotechnology Magazine, 2013, 12, 203-214.	1.1	9
60	Clocking with no field. Nature Nanotechnology, 2014, 9, 14-15.	15.6	9
61	A Flash-Based Multi-Bit Content-Addressable Memory with Euclidean Squared Distance. , 2021, , .		9
62	Application-driven Design Exploration for Dense Ferroelectric Embedded Non-volatile Memories. , 2021, , .		9
63	Can Beyond-CMOS Devices Illuminate Dark Silicon?. , 2016, , .		9
64	Defect tolerance in QCA-based PLAs. , 2008, , .		8
65	A Nanomagnet Logic Field-Coupled Electrical Input. IEEE Nanotechnology Magazine, 2013, 12, 734-742.	1.1	8
66	Error analysis for ultra dense nanomagnet logic circuits. Journal of Applied Physics, 2015, 117, .	1.1	8
67	ICCAD Tutorial Session Paper Ferroelectric FET Technology and Applications: From Devices to Systems. , 2021, , .		8
68	Power reduction in nanomagnet logic using high-permeability dielectrics. Journal of Applied Physics, 2013, 113, 17B906.	1.1	6
69	TFET-based Operational Transconductance Amplifier Design for CNN Systems. , 2015, , .		6
70	Design of Stochastic Computing Circuits Using Nanomagnetic Logic. IEEE Nanotechnology Magazine, 2016, 15, 179-187.	1.1	6
71	Design Tradeoffs for Improved Performance in MQCA-Based Systems. , 2008, , .		5
72	GPU acceleration of Data Assembly in Finite Element Methods and its energy implications. , 2013, , .		5

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73	Cross-layer efforts for energy-efficient computing: towards peta operations per second per watt. Frontiers of Information Technology and Electronic Engineering, 2018, 19, 1209-1223.	1.5	5
74	Energy-Efficient Convolutional Neural Network Based on Cellular Neural Network Using Beyond-CMOS Technologies. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 85-93.	1.1	5
75	Ferroelectric FET Based TCAM Designs for Energy Efficient Computing. , 2019, , .		5
76	A Fast and Energy Efficient Computing-in-Memory Architecture for Few-Shot Learning Applications. , 2020, , .		5
77	Computing-In-Memory Using Ferroelectrics: From Single- to Multi-Input Logic. IEEE Design and Test, 2022, 39, 56-64.	1.1	5
78	Design of Latches and Flip-Flops using Emerging Tunneling Devices. , 2016, , .		5
79	Nanomagnet Logic Gate With Programmable-Electrical Input. IEEE Transactions on Magnetics, 2014, 50, 1-4.	1.2	4
80	Analytically modeling power and performance of a CNN system. , 2015, , .		4
81	Can beyond-CMOS devices illuminate dark silicon?. Communications of the ACM, 2018, 61, 60-69.	3.3	4
82	Modeling and Design for Magnetoelectric Ternary Content Addressable Memory (TCAM). IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2022, 8, 44-52.	1.1	4
83	Cellular neural networks for image analysis using steep slope devices. , 2014, , .		3
84	Impact of steep-slope transistors on non-von Neumann architectures: CNN case study. , 2014, , .		3
85	Biomedical Image Segmentation Using Fully Convolutional Networks on TrueNorth. , 2018, , .		3
86	Impact of steep-slope transistors on non-von Neumann architectures: CNN case study. , 2014, , .		3
87	A Device Non-Ideality Resilient Approach for Mapping Neural Networks to Crossbar Arrays. , 2020, , .		3
88	AxR-NN: Approximate Computation Reuse for Energy-Efficient Convolutional Neural Networks. , 2020, , .		3
89	IMCRYPTO: An In-Memory Computing Fabric for AES Encryption and Decryption. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2022, 30, 553-565.	2.1	3
90	Eva-CAM: A Circuit/Architecture-Level Evaluation Tool for General Content Addressable Memories. , 2022, , .		3

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91	Systematic Design of Nanomagnet Logic Circuits. , 2013, , .		2
92	Exploiting Non-Volatility for Information Processing. , 2017, , .		2
93	Nonvolatile Spintronic Memory Cells for Neural Networks. IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, 2019, 5, 67-73.	1.1	2
94	An Energy Efficient Non-Volatile Flip-Flop based on CoMET Technology. , 2019, , .		2
95	The Implications of Ferroelectric FET Device Models to the Design of Computing-in-Memory Architectures. Journal of Integrated Circuits and Systems, 2021, 16, 1-8.	0.3	2
96	Cross-layer Design for Computing-in-Memory. , 2021, , .		2
97	Hardware-Software Co-Design of an In-Memory Transformer Network Accelerator. Frontiers in Electronics, 2022, 3, .	2.0	2
98	Power reduction in nanomagnetic logic clocking through high permeability dielectrics. , 2012, , .		1
99	Design of 3D nanomagnetic logic circuits: A full-adder case study. , 2014, , .		1
100	Contiguous clock lines for pipelined nanomagnet logic. Journal of Computational Electronics, 2014, 13, 763-768.	1.3	1
101	A CNN-Inspired Mixed Signal Processor Based on Tunnel Transistors. , 2015, , .		1
102	Fabrication of pseudo-spin-valve giant magnetoresistance arrays for nanomagnet logic by liftoff and the snow-jet process. Journal of Vacuum Science and Technology B:Nanotechnology and Microelectronics, 2015, 33, 022801.	0.6	1
103	Exploiting FeFETs via Cross-Layer Design from In-memory Computing Circuits to Meta-Learning Applications. , 2021, , .		1
104	Towards Systematic Design of 3D pNML Layouts. , 2015, , .		0
105	Guest Editorsâ€™ Introduction: Special Issue on Architecture Advances Enabled by Emerging Technologies. IEEE Design and Test, 2019, 36, 5-6.	1.1	0
106	Design of 3D nanomagnetic logic circuits: A full-adder case study. , 2014, , .		0