Kong-Pang Pun

List of Publications by Year
in descending order

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115	970	623574	580701
papers	citations	14 h-index	25 g-index

115	115	115	776
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 0.59-mW 78.7-dB SNDR 2-MHz Bandwidth Active-RC Delta-Sigma Modulator With Relaxed and Reduced Amplifiers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1114-1122.	3.5	5
2	A 270 nW Switched-Capacitor Acoustic Feature Extractor for Always-On Voice Activity Detection. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1045-1054.	3.5	15
3	A Current-Switching Technique for Intra-Body Communication with Miniaturized Electrodes. IEEE Transactions on Biomedical Circuits and Systems, 2021, PP, 1-1.	2.7	0
4	A Capacitor-Reused 2b/Cycle Active-Passive Second-order Noise-Shaping SAR ADC. Solid State Electronics Letters, 2021, 3, 27-31.	1.0	0
5	A 9.6 nW, 8-Bit, 100 S/s Envelope-to-Digital Converter for Respiratory Monitoring. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 445-449.	2.2	4
6	A Power-Efficient 10-MHz Bandwidth Active-RC CTDSM with a Charge-Recycled Highly-Linear 5-Level SC DAC. , 2020, , .		0
7	A 0.032-mm2 43.3-fJ/Step 100â€“200-MHz IF 2-MHz Bandwidth Bandpass DSM Based on Passive N-Path Filters. IEEE Journal of Solid-State Circuits, 2020, 55, 2443-2455.	3.5	6
8	An Extremely Linear Multi-Level DAC for Continuous-Time Delta-Sigma Modulators. IEEE Transactions on Circuits and Systems II: Express Briefs, 2019, 66, 367-371.	2.2	6
9	A DEM-Free Sturdy MASH Delta-Sigma Modulator with a Highly-Linear Tri-level DAC. , 2019, , .		1
10	A Highly Linear Multi-Level SC DAC in a Power-Efficient Gm-C Continuous-Time Delta-Sigma Modulator. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4592-4605.	3.5	11
11	A 0.4-V 0.2 pJ/step 90-dB SNDR 20-kHz CT delta-sigma modulator using class-AB amplifier with a novel local common-mode feedback. IEICE Electronics Express, 2019, 16, 20190170-20190170.	0.3	4
12	An Automatic On-Chip Calibration Technique for Static and Dynamic DAC Error Correction in High-Speed Continuous-Time Delta-Sigma Modulators. IEEE Access, 2019, 7, 172097-172109.	2.6	1
13	Power-Efficient Gm-C DSMs With High Immunity to Aliasing, Clock Jitter, and ISI. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 337-349.	2.1	6
14	Improving Power Efficiency for Active-<italic>RC</italic> Delta-Sigma Modulators Using a Passive-<italic>RC</italic> Low-Pass Filter in the Feedback. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1559-1563.	2.2	14
15	Low-Cost Maximum Efficiency Tracking Method For Wireless Power Transfer Systems. IEEE Transactions on Power Electronics, 2018, 33, 5317-5329.	5.4	52
16	A Self-Clocked Resistive CMOS Smart Temperature Sensor for Wireless Sensor Networks. Journal of Circuits, Systems and Computers, 2018, 27, 1850091.	1.0	2
17	A Gm-C Delta-Sigma Modulator With a Merged Input-Feedback Gm Circuit for Nonlinearity Cancellation and Power Efficiency Enhancement. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 1196-1209.	3.5	13
18	Power-Efficient Active-RC CT DSM with a Lowpass Capacitor at the Virtual Ground Node of the First Integrator. , 2018, , .		4

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19	An SAR ADC Switching Scheme With MSB Prediction for a Wide Input Range and Reduced Reference Voltage. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2863-2872.	2.1	6
20	A 24-kHz third-order continuous-time delta-sigma modulator using passive LPF. , 2017, , .		0
21	Reduction of clock jitter effect in 1-bit CT delta-sigma modulators by correlated clocks. , 2017, , .		0
22	Active-RC continuous-time DSM with FIR+SCR DAC. , 2017, , .		0
23	Continuous-time delta-sigma modulator with an upfront passive-RC low-pass network. , 2017, , .		6
24	A fast three-level feedback technique in continuous-time delta-sigma modulators. , 2016, , .		0
25	An 11b 40MS/s charge pump and comparator based pipelined ADC with variable reset voltages. , 2016, , .		1
26	A 25-kHz 3rd-order continuous-time Delta-Sigma modulator using tri-level quantizer. , 2016, , .		0
27	Gm-cell nonlinearity compensation technique using single-bit quantiser and FIR DAC in Gm-C based delta-sigma modulators. , 2016, , .		3
28	A 10-bit 2 MS/s SAR ADC using reverse VCM-based switching scheme. , 2016, , .		5
29	Guest Editorial: Next-Generation Delta-Sigma Converters. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 481-483.	2.7	0
30	An efficient frequency compensation scheme for CMFB loop in fully differential amplifiers. , 2015, , .		4
31	A 5.4-mW 180-cm Transmission Distance 2.5-Mb/s Advanced Techniques-Based Novel Intrabody Communication Receiver Analog Front End. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 2829-2841.	2.1	13
32	Next-Generation Delta-Sigma Converters: Trends and Perspectives. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2015, 5, 484-499.	2.7	64
33	A Charge Recycling SAR ADC With a LSB-Down Switching Scheme. IEEE Transactions on Circuits and Systems I: Regular Papers, 2015, 62, 356-365.	3.5	36
34	A Resistor-Based Sub-1-V CMOS Smart Temperature Sensor for VLSI Thermal Management. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1651-1660.	2.1	20
35	Capacitive digitalâ€toâ€analogue converters with least significant bit down in differential successive approximation register ADCs. Journal of Engineering, 2014, 2014, 45-48.	0.6	1
36	Optimizing the Stage Resolution in Pipelined SAR ADCs for High-Speed High-Resolution Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2014, 61, 476-480.	2.2	14

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37	A High-Linearity Capacitance-to-Digital Converter Suppressing Charge Errors From <newline/>Bottom-Plate Switches. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 1928-1941.	3.5	16
38	23 ÂµW 8.9â€effective number of bit 1.1ÂMS/s successive approximation register analogâ€toâ€digital converter with an energyâ€efficient digitalâ€toâ€analog converter switching scheme. Journal of Engineering, 2014, 2014, 420-425.	0.6	0
39	Architecture and Design Flow for a Highly Efficient Structured ASIC. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 424-433.	2.1	14
40	Unit capacitor array based SAR ADC. Microelectronics Reliability, 2013, 53, 505-508.	0.9	11
41	A 0.9V 5kS/s resistor-based time-domain temperature sensor in 90nm CMOS with calibrated inaccuracy of −0.6°C/0.8°C from −40°C to 125°C. , 2013, , .		5
42	Novel overshoot cancellation in comparator-based pipelined ADC. , 2012, , .		4
43	Analysis and Design of a 14-bit SAR ADC using self-calibration DAC. , 2012, , .		3
44	Low-offset comparator using capacitive self-calibration. , 2012, , .		7
45	A 0.5-V 90-dB SNDR 102ÂdB-SFDR audio-band continuous-time deltaâ€“sigma modulator. Analog Integrated Circuits and Signal Processing, 2012, 71, 159-169.	0.9	5
46	Vernier parallel delay-line based time-to-digital converter. Analog Integrated Circuits and Signal Processing, 2012, 71, 151-153.	0.9	2
47	A 0.5ÂV 65.7ÂdB 1ÂMHz continuous-time complex delta sigma modulator. Analog Integrated Circuits and Signal Processing, 2011, 66, 255-267.	0.9	4
48	A 0.5-V 81.2 dB SNDR audio-band continuous-time Delta-Sigma modulator with SCR feedback. Analog Integrated Circuits and Signal Processing, 2011, 67, 285-292.	0.9	6
49	A NOVEL SWITCHED-CURRENT SUCCESSIVE APPROXIMATION ADC. Journal of Circuits, Systems and Computers, 2011, 20, 15-27.	1.0	7
50	A low voltage current mode CMOS integrated receiver front-end for GPS system. Analog Integrated Circuits and Signal Processing, 2010, 63, 23-31.	0.9	9
51	Structured ASIC: Methodology and comparison. , 2010, , .		3
52	A 0.5V 2-1 cascaded continuous-time Delta-Sigma modulator synthesized with a new method. , 2010, , .		1
53	A 0.5-Hz High-Pass Cutoff Dual-Loop Transimpedance Amplifier for Wearable NIR Sensing Device. IEEE Transactions on Circuits and Systems II: Express Briefs, 2010, 57, 531-535.	2.2	15
54	A Low-Power Continuously-Calibrated Clock Recovery Circuit for UHF RFID EPC Class-1 Generation-2 Transponders. IEEE Journal of Solid-State Circuits, 2010, 45, 587-599.	3.5	24

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55	A 90nm RFID tag's baseband processor with novel PIE decoder and uplink clock generator. , 2010, , .		11
56	A 0.4 V low power baseband processor for UHF passive RFID tags. , 2010, , .		6
57	Design of a single layer programmable Structured ASIC library. , 2010, , .		5
58	Analysis of the behaviours of phase and amplitude mismatch compensators to achieve 82.5 dB image rejection ratio. International Journal of Electronics, 2010, 97, 553-568.	0.9	0
59	A 0.5V amplifier with adaptive CMFB compensation for a 2-1 cascade CT Delta Sigma modulator. , 2010, , .		1
60	Rapid prototyping on a structured ASIC fabric. , 2010, , .		2
61	A Low-power signal processing front-end and decoder for UHF passive RFID transponders. , 2009, , .		6
62	A novel mismatch cancellation and I/Q channel multiplexing scheme for quadrature bandpass ΔΣ modulators. , 2009, , .		2
63	A dynamic element matching technique for multi-bit quadrature delta-sigma modulators. , 2009, , .		0
64	A 0.5-V Wideband Amplifier for a 1-MHz CT Complex Delta-Sigma Modulator. IEEE Transactions on Circuits and Systems II: Express Briefs, 2009, 56, 805-809.	2.2	16
65	A passive RFID tag IC development platform. , 2009, , .		0
66	A 1.2-V single-sideband upconverter system with high spurious suppression for UWB frequency synthesizers. , 2009, , .		2
67	A quaternary current mode bus driver and receiver circuits. , 2009, , .		0
68	A 4-GHz VCO for Multiband OFDM UWB systems. , 2008, , .		1
69	Design of passive UHF RFID tag in 130nm CMOS technology. , 2008, , .		14
70	A Fully Differential Band-Selective Low-Noise Amplifier for MB-OFDM UWB Receivers. IEEE Transactions on Circuits and Systems II: Express Briefs, 2008, 55, 653-657.	2.2	22
71	Design and challenges of passive UHF RFID tag in 90nm CMOS technology. , 2008, , .		1
72	Enhanced channel selection using digital low-IF in Weaver receiver architecture. , 2008, , .		1

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73	A 6-digit RSD analog-to-quaternary converter with CMOS Current Mode Quaternary Adders. , 2007, , .		1
74	A 0.5-V 74-dB SNDR 25-kHz Continuous-Time Delta-Sigma Modulator With a Return-to-Open DAC. IEEE Journal of Solid-State Circuits, 2007, 42, 496-507.	3.5	104
75	Correction to â€œA 0.5-V 74-dB SNDR 25-kHz Continuous-Time Delta-Sigma Modulator With a Return-to-Open DACâ€• IEEE Journal of Solid-State Circuits, 2007, 42, 2315-2315.	3.5	1
76	A low power CMOS front-end for photoplethysmongraphic signal acquisition with robust DC Photocurrent Rejection. , 2007, , .		2
77	Power-Efficient VLSI Realization of a Complex FSM for H.264/AVC Bitstream Parsing. IEEE Transactions on Circuits and Systems II: Express Briefs, 2007, 54, 984-988.	2.2	3
78	A DEM Scheme for I/Q Mismatch Compensation in Multi-Bit CT Î”Î£ Modulator. , 2007, , .		1
79	Design challenges of voltage multiplier in a 0.35-μm 2-poly 4-metal CMOS technology for RFID passive tags. , 2007, , .		0
80	A Speech Recognition IC Using Hidden Markov Models with Continuous Observation Densities. Journal of Signal Processing Systems, 2007, 47, 223-232.	1.0	4
81	Sub-1 V Current Mode CMOS Integrated Receiver Front-end for GPS System. , 2006, , .		0
82	Adiabatic Smart Card. , 2006, , .		9
83	0.8 V GPS band CMOS VCO with 29% Tuning Range. , 2006, , .		2
84	A 75-dB Image Rejection IF-Input Quadrature-Sampling SC<tex>$SigmaDelta$</tex>Modulator. IEEE Journal of Solid-State Circuits, 2006, 41, 1353-1363.	3.5	8
85	A Sub-1 V 1.6 GHz CMOS VCO with 29% Tuning Range. , 2006, , .		1
86	A NIR CMOS preamplifier with DC photocurrent rejection for pulsed light source. , 2006, , .		2
87	Current-Division-Based Digital Frequency Tuning for Active RC Filters. Analog Integrated Circuits and Signal Processing, 2005, 45, 61-69.	0.9	6
88	A finger-tracking virtual mouse realized in an embedded system. , 2005, , .		7
89	An I/Q Mismatch-Free Switched-Capacitor Complex Sigmaâ€“Delta Modulator. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 254-256.	2.3	12
90	A Low-Latency Asynchronous Shift Register. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2004, 51, 217-221.	2.3	3

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91	Quadrature sampling schemes with improved image rejection. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2003, 50, 641-648.	2.3	16
92	Reversed nested miller compensation with voltage buffer and nulling resistor. IEEE Journal of Solid-State Circuits, 2003, 38, 1735-1738.	3.5	76
93	A CMOS current feedback operational amplifier with active current mode compensation. , 0, , .		0
94	A 1.2 V 900 MHz CMOS mixer. , 0, , .		13
95	A low power asynchronous GF(2/sup 173/) ALU for elliptic curve crypto-processor. , 0, , .		7
96	An HMM-based speech recognition IC. , 0, , .		13
97	Clock recovery circuit with adiabatic technology (quasi-static CMOS logic). , 0, , .		5
98	A 1 V 1.1 GHz CMOS integrated receiver front-end. , 0, , .		0
99	An asynchronous SOVA decoder for wireless communication application. , 0, , .		3
100	A low power asynchronous java processor for contactless smart card. , 0, , .		0
101	A sub-harmonic oscillator using an injection-locked DCO. , 0, , .		0
102	A new current mirror memory cell to improve the power efficiency of CMOS current mode analog circuits. , 0, , .		1
103	CMOS RF LNA with high ESD immunity. , 0, , .		4
104	Ramp Voltage Supply using Adiabatic Charging Principle. , 0, , .		0
105	A Near-Infrared Heart Rate Sensor IC With Very Low Cutoff Frequency using Current Steering Technique. , 0, , .		2
106	A Speech Recognizer With Selectable Model Parameters. , 0, , .		1
107	Realization of Card-Centric Framework: A Card-Centric Computer. , 0, , .		0
108	Active RC Filter with Reduced Capacitance by Current Division Technique. , 0, , .		1

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109	A 75dB image rejection IF-input quadrature sampling SC ΣΔ modulator. , 0, , .		0
110	A 0.5V Fully Differential OTA with Local Common Feedback. , 0, , .		3
111	An optimal normal basis elliptic curve cryptoprocessor for inductive RFID application. , 0, , .		0
112	An efficient MFCC extraction method in speech recognition. , 0, , .		112
113	A 6-digit CMOS Current-Mode Analog-to-Quaternary Converter with RSD Error Correction Algorithm. , 0, , .		2
114	A fully differential low noise amplifier with real-time channel hopping for ultra-wideband wireless applications. , 0, , .		2
115	A passive secondâ€order noiseâ€shaping SAR ADC architecture with increased freedom in NTF synthesis and relaxed clockâ€jitter issue. Electronics Letters, 0, , .	0.5	0