Shuvra S Bhattacharyya

List of Publications by Year in Descending Order

218 papers	1,865 citations	20 h-index	34 g-index
265 ext. papers	2,257 ext. citations	2.5 avg, IF	4.92 L-index

#	Paper	IF	Citations
218	VR-PRUNE: Decidable Variable-Rate Dataflow for Signal Processing Systems. *IEEE Transactions on Signal Processing*, **2022**, 1-1	4.8	
217	A Framework for Fixed Priority Periodic Scheduling Synthesis from Synchronous Data-Flow Graphs. *Lecture Notes in Computer Science*, **2022**, 259-271	0.9	
216	Multimedia Content Analysis with Dynamic Data Driven Applications Systems (DDDAS) **2022**, 645-667		
215	Design of a Dynamic Data-Driven System for Multispectral Video Processing **2022**, 539-556		
214	Rapid Quality Assessment of Nonrigid Image Registration Based on Supervised Learning. *Journal of Digital Imaging*, **2021**, 34, 1376	5.3	
213	Neural decoding on imbalanced calcium imaging data with a network of support vector machines. *Advanced Robotics*, **2021**, 35, 459-470	1.7	0
212	Hyperspectral Image Classification With Attention-Aided CNNs. *IEEE Transactions on Geoscience and Remote Sensing*, **2021**, 59, 2281-2293	8.1	89
211	CGMBE: a model-based tool for the design and implementation of real-time image processing applications on CPU GPU platforms. *Journal of Real-Time Image Processing*, **2021**, 18, 561-583	1.9	0
210	Software synthesis from dataflow schedule graphs. *SN Applied Sciences*, **2021**, 3, 1	1.8	0
209	A novel view synthesis approach based on view space covering for gait recognition. *Neurocomputing*, **2021**, 453, 13-25	5.4	3
208	PathTracing: Raising the Level of Understanding of Processing Latency in Heterogeneous MPSoCs **2021**,		2
207	PathTracer: Understanding Response Time of Signal Processing Applications on Heterogeneous MPSoCs. *ACM Transactions on Modeling and Performance Evaluation of Computing Systems*, **2021**, 6, 1-30	0.8	
206	Decidable Variable-Rate Dataflow for Heterogeneous Signal Processing Systems **2020**,		1
205	Real-Time Neuron Detection and Neural Signal Extraction Platform for Miniature Calcium Imaging. *Frontiers in Computational Neuroscience*, **2020**, 14, 43	3.5	1
204	Prinet: A Prior Driven Spectral Super-Resolution Network **2020**,		4
203	Spectral Super Resolution with DCT Decomposition and Deep Residual Learning. *Lecture Notes in Computer Science*, **2020**, 171-178	0.9	
202	Scheduling of Synchronous Dataflow Graphs with Partially Periodic Real-Time Constraints **2020**,		2

201	Runtime Adaptation in Wireless Sensor Nodes Using Structured Learning. *ACM Transactions on Cyber-Physical Systems*, **2020**, 4, 1-28	2.3	1
200	Dynamic, Data-Driven Hyperspectral Image Classification on Resource-Constrained Platforms. *Lecture Notes in Computer Science*, **2020**, 320-327	0.9	0
199	. *Computer*, **2020**, 53, 71-75	1.6	2
198	Passive-Active Flowgraphs for Efficient Modeling and Design of Signal Processing Systems. *Journal of Signal Processing Systems*, **2020**, 92, 1133-1151	1.4	
197	Rotators in Fast Fourier Transforms **2020**, 245-262		
196	WGEVIA: A Graph Level Embedding Method for Microcircuit Data. *Frontiers in Computational Neuroscience*, **2020**, 14, 603765	3.5	
195	Gradient Image Super-resolution for Low-resolution Image Recognition **2019**,		3
194	Design Space Exploration for Wireless-Integrated Factory Automation Systems **2019**,		1
193	Multi-Scale Gradient Image Super-Resolution for Preserving SIFT Key Points in Low-Resolution Images. *Signal Processing: Image Communication*, **2019**, 78, 236-245	2.8	5
192	Optimized implementation of digital signal processing applications with gapless data acquisition. *Eurasip Journal on Advances in Signal Processing*, **2019**, 2019,	1.9	1
191	Multi-Frame Super Resolution with Deep Residual Learning on Flow Registered Non-Integer Pixel Images **2019**,		2
190	Segmentation of surgical instruments in laparoscopic videos: training dataset generation and deep-learning-based framework **2019**,		3
189	Dynamic Dataflow Graphs **2019**, 1173-1210		3
188	GEMBench: A Platform for Collaborative Development of GPU Accelerated Embedded Markov Decision Systems. *Lecture Notes in Computer Science*, **2019**, 294-308	0.9	
187	Hyperspectral Video Processing on Resource-Constrained Platforms **2019**,		1
186	Weakly supervised segmentation for real-time surgical tool tracking. *Healthcare Technology Letters*, **2019**, 6, 231-236	1.9	4
185	Real-Time Calcium Imaging Based Neural Decoding with a Support Vector Machine **2019**,		3
184	MADS: A Framework for Design and Implementation of Adaptive Digital Predistortion Systems. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2019**, 9, 712-722	5.2	2

183	An integrated hardware/software design methodology for signal processing systems. *Journal of Systems Architecture*, **2019**, 93, 1-19	5.5	10
182	Model-Based Dynamic Scheduling for Multicore Signal Processing. *Journal of Signal Processing Systems*, **2019**, 91, 981-994	1.4	
181	Reconfigurable Digital Channelizer Design Using Factored Markov Decision Processes. *Journal of Signal Processing Systems*, **2018**, 90, 1329-1343	1.4	3
180	A design tool for high performance image processing on multicore platforms **2018**,		1
179	Reproducible Evaluation of System Efficiency With a Model of Architecture: From Theory to Practice. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2050-2063	2.5	10
178	Model-Based Representations for Dataflow Schedules. *Lecture Notes in Computer Science*, **2018**, 88-105	0.9	1
177	Memory-Constrained Vectorization and Scheduling of Dataflow Graphs for Hybrid CPU-GPU Platforms. *Transactions on Embedded Computing Systems*, **2018**, 17, 1-25	1.8	4
176	Dynamic Data Driven Application Systems (DDDAS) for Multimedia Content Analysis **2018**, 631-651		
175	Design of a Dynamic Data-Driven System for Multispectral Video Processing **2018**, 529-545		1
174	PRUNE: Dynamic and Decidable Dataflow for Signal Processing on Heterogeneous Platforms. *IEEE Transactions on Signal Processing*, **2018**, 66, 654-665	4.8	7
173	Elastic Neural Networks: A Scalable Framework for Embedded Computer Vision **2018**,		5
172	Generalized Graph Connections for Dataflow Modeling of DSP Applications **2018**,		2
171	Efficient Solving of Markov Decision Processes on GPUs Using Parallelized Sparse Matrices **2018**,		5
170	Model-based cosimulation for industrial wireless networks **2018**,		4
169	Implementation, Scheduling, and Adaptation of Partial Expansion Graphs on Multicore Platforms. *Journal of Signal Processing Systems*, **2017**, 87, 107-125	1.4	5
168	Data Flow Algorithms for Processors with Vector Extensions. *Journal of Signal Processing Systems*, **2017**, 87, 21-31	1.4	1
167	Implementation of a Multirate Resampler for Multi-carrier Systems on GPUs. *Journal of Signal Processing Systems*, **2017**, 89, 445-455	1.4	0
166	Introduction to Hardware/Software Codesign **2017**, 3-26		0

165	Online learning in neural decoding using incremental linear discriminant analysis **2017**,		6
164	A Hybrid Task Graph Scheduler for High Performance Image Processing Workflows. *Journal of Signal Processing Systems*, **2017**, 89, 457-467	1.4	5
163	An accumulative fusion architecture for discriminating people and vehicles using acoustic and seismic signals **2017**,		7
162	Hardware design methodology using lightweight dataflow and its integration with low power techniques. *Journal of Systems Architecture*, **2017**, 78, 15-29	5.5	4
161	An optimized embedded target detection system using acoustic and seismic sensors **2017**,		3
160	Low-power heterogeneous computing via adaptive execution of dataflow actors **2017**,		1
159	Dynamic, data-driven processing of multispectral video streams. *IEEE Aerospace and Electronic Systems Magazine*, **2017**, 32, 50-57	2.4	9
158	Model-based dynamic scheduling for multicore implementation of image processing systems **2017**,		2
157	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems **2017**, 1185-1219		9
156	Scheduling of Parallelized Synchronous Dataflow Actors for Multicore Signal Processing. *Journal of Signal Processing Systems*, **2016**, 83, 309-328	1.4	0
155	Jitter measurement on deep waveforms with constant memory **2016**,		1
154	Evolutionary Multiobjective Optimization for Digital Predistortion Architectures. *Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering*, **2016**, 498-510	0.2	2
153	Instrumentation-Driven Validation of Dataflow Applications. *Journal of Signal Processing Systems*, **2016**, 84, 383-397	1.4	
152	A Wideband Front-End Receiver Implementation on GPUs. *IEEE Transactions on Signal Processing*, **2016**, 64, 2602-2612	4.8	3
151	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems **2016**, 1-35		3
150	Compact modeling and management of reconfiguration in digital channelizer implementation **2016** ,		5
149	Resource-constrained implementation and optimization of a deep neural network for vehicle classification **2016**,		5
148	Models of Architecture: Reproducible Efficiency Evaluation for Signal Processing Systems **2016**,		4

147	A Design Framework for Mapping Vectorized Synchronous Dataflow Graphs onto CPU-GPU Platforms **2016**,		3
146	Parameterized Sets of Dataflow Modes And Their Application to Implementation of Cognitive Radio Systems. *Journal of Signal Processing Systems*, **2015**, 80, 3-18	1.4	10
145	Constant-rate clock recovery and jitter measurement on deep memory waveforms using dataflow **2015**,		4
144	Multiobjective Design Optimization in the Lightweight Dataflow for DDDAS Environment (LiD4E) 1. *Procedia Computer Science*, **2015**, 51, 2563-2572	1.6	4
143	A hybrid task graph scheduler for high performance image processing workflows **2015**,		5
142	An efficient GPU implementation of a multirate resampler for multi-carrier systems **2015**,		1
141	Model-based design and implementation of an adaptive digital predistortion filter **2015**,		2
140	Mapping Parameterized Dataflow Graphs onto FPGA Platforms. *Academic Press Library in Signal Processing*, **2014**, 4, 643-673		1
139	Model Based Design Environment for Data-driven Embedded Signal Processing Systems1. *Procedia Computer Science*, **2014**, 29, 1193-1202	1.6	5
138	Instrumentation-driven framework for validation of dataflow applications **2014**,		1
137	Implementation of a high-throughput low-latency polyphase channelizer on GPUs. *Eurasip Journal on Advances in Signal Processing*, **2014**, 2014,	1.9	5
136	Low-Complexity Digital Predistortion for Reducing Power Amplifier Spurious Emissions in Spectrally-Agile Flexible Radio **2014**,		7
135	Data flow algorithms for processors with vector extensions: Handling actors with internal state **2014**,		1
134	Partial expansion of dataflow graphs for resource-aware scheduling of multicore signal processing systems **2014**,		1
133	Low power implementation of digital predistortion filter on a heterogeneous application specific multiprocessor **2014**,		6
132	Efficient architecture mapping of FFT/IFFT for cognitive radio networks **2014**,		6
131	Implementation of a low-complexity low-latency arbitrary resampler on GPUs **2014**,		5
130	Just-in-time scheduling techniques for multicore signal processing systems **2014**,		4

129	Dynamic, data-driven spectrum management in cognitive small cell networks **2014**,		1
128	Data-Driven Stream Mining Systems for Computer Vision. *Advances in Computer Vision and Pattern Recognition*, **2014**, 249-264	1.1	2
127	Dataflow-Based, Cross-Platform Design Flow for DSP Applications. *Embedded Systems*, **2014**, 41-65		1
126	Parameterized Scheduling of Topological Patterns in Signal Processing Dataflow Graphs. *Journal of Signal Processing Systems*, **2013**, 71, 275-286	1.4	1
125	A Design Methodology for Distributed Adaptive Stream Mining Systems. *Procedia Computer Science* , **2013**, 18, 2482-2491	1.6	1
124	A novel framework for design and implementation of adaptive stream mining systems **2013**,		4
123	PiMM: Parameterized and Interfaced dataflow Meta-Model for MPSoCs runtime reconfiguration **2013**,		39
122	Scheduling of parallelized synchronous dataflow actors **2013**,		2
121	Integration of Dataflow-Based Heterogeneous Multiprocessor Scheduling Techniques in GNU Radio. *Journal of Signal Processing Systems*, **2013**, 70, 177-191	1.4	10
120	High-performance and low-energy buffer mapping method for multiprocessor DSP systems. *Transactions on Embedded Computing Systems*, **2013**, 12, 1-23	1.8	2
119	Configurable, resource-optimized FFT architecture for OFDM communication **2013**,		1
118	**2013**,		12
117	Pipelined FFT for wireless communications supporting 128□2048 / 1536 -point transforms **2013**,		5
116	Instrumentation-Driven Model Detection and Actor Partitioning for Dataflow Graphs. *International Journal of Embedded and Real-Time Communication Systems*, **2013**, 4, 1-21	0.6	2
115	Dynamic Dataflow Graphs **2013**, 905-944		13
114	Mapping Parameterized Cyclo-static Dataflow Graphs onto Configurable Hardware. *Journal of Signal Processing Systems*, **2012**, 66, 285-301	1.4	8
113	. *IEEE Transactions on Multimedia*, **2012**, 14, 630-640	6.6	6
112	Multidimensional Dataflow Graph Modeling and Mapping for Efficient GPU Implementation **2012**,		1

111	Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications **2012**,		5
110	Parameterized scheduling for signal processing systems using topological patterns **2012**,		2
109	Overview of the MPEG Reconfigurable Video Coding Framework. *Journal of Signal Processing Systems*, **2011**, 63, 251-263	1.4	51
108	Exploiting Statically Schedulable Regions in Dataflow Programs. *Journal of Signal Processing Systems*, **2011**, 63, 129-142	1.4	15
107	Topological Patterns for Scalable Representation and Analysis of Dataflow Graphs. *Journal of Signal Processing Systems*, **2011**, 65, 229-244	1.4	4
106	Vectorization and mapping of software defined radio applications on heterogeneous multi-processor platforms **2011**,		4
105	A Model-Based Schedule Representation for Heterogeneous Mapping of Dataflow Graphs **2011**,		8
104	Design methods for Wireless Sensor Network Building Energy Monitoring Systems **2011**,		2
103	Applying graphics processor acceleration in a software defined radio prototyping environment **2011**,		7
102	Multithreaded Simulation for Synchronous Dataflow Graphs. *ACM Transactions on Design Automation of Electronic Systems*, **2011**, 16, 1-23	1.5	2
101	The DSPCAD Integrative Command Line Environment: Introduction to DICE Version 1.1 **2011**,		3
100	Heterogeneous Design in Functional DIF. *Lecture Notes in Computer Science*, **2011**, 391-408	0.9	3
99	Simulating dynamic communication systems using the core functional dataflow model **2010**,		2
98	Efficient static buffering to guarantee throughput-optimal FPGA implementation of synchronous dataflow graphs **2010**,		3
97	Automated generation of an efficient MPEG-4 Reconfigurable Video Coding decoder implementation **2010**,		1
96	Energy-driven distribution of signal processing applications across wireless sensor networks. *ACM Transactions on Sensor Networks*, **2010**, 6, 1-32	2.9	7
95	Analysis of SystemC actor networks for efficient synthesis. *Transactions on Embedded Computing Systems*, **2010**, 10, 1-34	1.8	9
94	. *IEEE Signal Processing Magazine*, **2010**, 27, 61-68	9.4	2

93	. *IEEE Signal Processing Magazine*, **2010**, 27, 20-21	9.4	4
92	Rapid prototyping for digital signal processing systems using Parameterized Synchronous Dataflow graphs **2010**,		1
91	FPGA-based design and implementation of the 3GPP-LTE physical layer using parameterized synchronous dataflow techniques **2010**,		9
90	Scalable representation of dataflow graph structures using topological patterns **2010**,		5
89	Loop transformations for interface-based hierarchies IN SDF graphs **2010**,		2
88	A Low-overhead Scheduling Methodology for Fine-grained Acceleration of Signal Processing Systems. *Journal of Signal Processing Systems*, **2010**, 60, 333-343	1.4	2
87	Design and implementation of embedded computer vision systems based on particle filters. *Computer Vision and Image Understanding*, **2010**, 114, 1203-1214	4.3	13
86	Dynamic and Multidimensional Dataflow Graphs **2010**, 899-930		3
85	Exploiting statically schedulable regions in dataflow programs **2009**,		17
84	A generalized scheduling approach for dynamic dataflow applications **2009**,		21
83	Improving the performance of active set based Model Predictive Controls by dataflow methods **2009**,		1
82	Dataflow-based implementation of model predictive control **2009**,		2
81	Mode grouping for more effective generalized scheduling of dynamic dataflow applications **2009**,		7
80	Resource-efficient acceleration of 2-dimensional Fast Fourier Transform computations on FPGAs **2009**,		7
79	Signal processing on platforms with multiple cores: Part 1 - Overview and methodologies [From the Guest Editors]. *IEEE Signal Processing Magazine*, **2009**, 26, 24-25	9.4	9
78	Exploring the Concurrency of an MPEG RVC Decoder Based on Dataflow Program Analysis. *IEEE Transactions on Circuits and Systems for Video Technology*, **2009**, 19, 1646-1657	6.4	12
77	Integration of Dataflow optimization techniques into a software radio design framework **2009**,		1
76	High-Performance Buffer Mapping to Exploit DRAM Concurrency in Multiprocessor DSP Systems **2009**,		4

75	Interface-based hierarchy for synchronous data-flow graphs **2009**,		19
74	An architectural level design methodology for smart camera applications. *International Journal of Embedded Systems*, **2009**, 4, 83	0.5	4
73	Design Methodology for Embedded Computer Vision Systems **2009**, 27-47		3
72	Advances in hardware design and implementation of signal processing systems [DSP Forum]. *IEEE Signal Processing Magazine*, **2008**, 25, 175-180	9.4	3
71	Multiobjective Optimization of FPGA-Based Medical Image Registration **2008**,		4
70	Systematic generation of FPGA-based FFT implementations. *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, **2008**,	1.6	4
69	Towards systematic exploration of tradeoffs for medical image registration on heterogeneous platforms **2008**,		6
68	An Optimized Message Passing Framework for Parallel Implementation of Signal Processing Applications **2008**,		1
67	Sensor Support Systems for Asymmetric Threat Countermeasures. *IEEE Sensors Journal*, **2008**, 8, 682-6924		3
66	A generalized static data flow clustering algorithm for mpsoc scheduling of multimedia applications **2008**,		28
65	OpenDF. *Computer Architecture News*, **2008**, 36, 29-35		43
64	Multithreaded simulation for synchronous dataflow graphs **2008**,		5
63	Parameterized design framework for hardware implementation of particle filters. *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, **2008**,	1.6	7
62	Functional DIF for Rapid Prototyping **2008**,		54
61	Design and optimization of a distributed, embedded speech recognition system. *Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on*, **2008**,		4
60	Multiobjective Optimization for Reconfigurable Implementation of Medical Image Registration. *International Journal of Reconfigurable Computing*, **2008**, 2008, 1-17	2.1	2
59	Memory-constrained Block Processing for DSP Software Optimization. *Journal of Signal Processing Systems*, **2008**, 50, 163-177	1.4	8
58	Introduction to the Special Issue on Embedded Computing Systems for DSP. *Journal of Signal Processing Systems*, **2008**, 50, 97-98	1.4	

57	Model-based mapping of reconfigurable image registration on FPGA platforms. *Journal of Real-Time Image Processing*, **2008**, 3, 149-162	1.9	10
56	Heterogeneous Design in Functional DIF. *Lecture Notes in Computer Science*, **2008**, 157-166	0.9	14
55	A taxonomy for medical image registration acceleration techniques **2007**,		5
54	Low-Overhead Run-Time Scheduling for Fine-Grained Acceleration of Signal Processing Systems. *Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on*, **2007**,		4
53	Beyond single-appearance schedules. *Transactions on Embedded Computing Systems*, **2007**, 6, 14	1.8	4
52	Efficient simulation of critical synchronous dataflow graphs. *ACM Transactions on Design Automation of Electronic Systems*, **2007**, 12, 1-28	1.5	8
51	Parameterized Looped Schedules for Compact Representation of Execution Sequences in DSP Hardware and Software Implementation. *IEEE Transactions on Signal Processing*, **2007**, 55, 3126-3138	4.8	23
50	Compact, Low Power Wireless Sensor Network System for Line Crossing Recognition **2007**,		1
49	Energy-Aware Data Compression for Wireless Sensor Networks **2007**,		8
48	Dataflow-Based Mapping of Computer Vision Algorithms onto FPGAs. *Eurasip Journal on Embedded Systems*, **2007**, 2007, 1-12	2	5
47	**2007**,		10
46	Towards a Heterogeneous Medical Image Registration Acceleration Platform **2007**,		6
45	The pipeline decomposition tree: **2006**,		4
44	Efficient simulation of critical synchronous dataflow graphs **2006**,		12
43	Model-Based Mapping of Image Registration Applications onto Configurable Hardware **2006**,		5
42	Register File Partitioning with Constraint Programming **2006**,		1
41	Configuration and Representation of Large-Scale Dataflow Graphs using the Dataflow Interchange Format. *Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on*, **2006**,		2
40	Dataflow Transformations in High-level DSP System Design **2006**,		5

39	A Communication Interface for Multiprocessor Signal Processing Systems **2006**,		4
38	Affine Nested Loop Programs and their Binary Parameterized Dataflow Graph Counterparts **2006**,		7
37	Efficient techniques for clustering and scheduling onto embedded multiprocessors. *IEEE Transactions on Parallel and Distributed Systems*, **2006**, 17, 667-680	3.7	33
36	**2006**,		3
35	Reconfigurable image registration on FPGA platforms **2006**,		5
34	Contention-conscious transaction ordering in multiprocessor DSP systems. *IEEE Transactions on Signal Processing*, **2006**, 54, 556-569	4.8	6
33	Memory-constrained Block Processing Optimization for Synthesis of DSP Software **2006**,		3
32	Analysis of Dataflow Programs with Interval-limited Data-rates. *Journal of Signal Processing Systems* , **2006**, 43, 247-258		3
31	Energy-Driven Partitioning of Signal Processing Algorithms in Sensor Networks. *Lecture Notes in Computer Science*, **2006**, 142-154	0.9	5
30	Joint application mapping/interconnect synthesis techniques for embedded chip-scale multiprocessors. *IEEE Transactions on Parallel and Distributed Systems*, **2005**, 16, 99-112	3.7	13
29	Modeling of Block-Based DSP Systems. *Journal of Signal Processing Systems*, **2005**, 40, 289-299		8
28	DSP address optimization using evolutionary algorithms **2005**,		3
27	Software synthesis from the dataflow interchange format **2005**,		45
26	Buffer merging□ powerful technique for reducing memory requirements of synchronous dataflow specifications. *ACM Transactions on Design Automation of Electronic Systems*, **2004**, 9, 212-237	1.5	26
25	The CBP Parameter: A Module Characterization Approach for DSP Software Optimization. *Journal of Signal Processing Systems*, **2004**, 38, 131-146		1
24	. *IEEE Transactions on Signal Processing*, **2004**, 52, 1209-1217	4.8	4
23	Systematic integration of parameterized local search into evolutionary algorithms. *IEEE Transactions on Evolutionary Computation*, **2004**, 8, 137-155	15.6	52
22	Compact Procedural Implementation in DSP Software Synthesis Through Recursive Graph Decomposition. *Lecture Notes in Computer Science*, **2004**, 47-61	0.9	6

21	DIF: An Interchange Format for Dataflow-Based Design Tools. *Lecture Notes in Computer Science*, **2004**, 423-432	0.9	8
20	Logic Foundry: Rapid Prototyping for FPGA-Based DSP Systems. *Eurasip Journal on Advances in Signal Processing*, **2003**, 2003, 1	1.9	2
19	Intermediate Representations for Design Automation of Multiprocessor DSP Systems. *Design Automation for Embedded Systems*, **2002**, 7, 307-323	0.6	33
18	High-Level Synthesis of DSP Applications Using Adaptive Negative Cycle Detection. *Eurasip Journal on Advances in Signal Processing*, **2002**, 2002, 1	1.9	
17	Generating Compact Code from Dataflow Specifications of Multirate Signal Processing Algorithms **2002**, 452-464		
16	Parameterized dataflow modeling for DSP systems. *IEEE Transactions on Signal Processing*, **2001**, 49, 2408-2421	4.8	170
15	Adaptive negative cycle detection in dynamic graphs **2001**,		5
14	Multidimensional Exploration of Software Implementations for DSP Algorithms. *Journal of Signal Processing Systems*, **2000**, 24, 83-98		9
13	Shared memory implementations of synchronous dataflow specifications **2000**,		2
12	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2000**, 8, 452-455	2.6	18
11	Synthesis of Embedded Software from Synchronous Dataflow Specifications. *Journal of Signal Processing Systems*, **1999**, 21, 151-166		109
10	. *IEEE Transactions on Signal Processing*, **1997**, 45, 1605-1618	4.8	12
9	Joint Minimization of Code and Data for Synchronous Dataflow Programs. *Formal Methods in System Design*, **1997**, 11, 41-70	1.4	31
8	APGAN and RPMC: Complementary Heuristics for Translating DSP Block Diagrams into Efficient Software Implementations. *Design Automation for Embedded Systems*, **1997**, 2, 33-60	0.6	24
7	Looped schedules for dataflow descriptions of multirate signal processing algorithms. *Formal Methods in System Design*, **1994**, 5, 183-205	1.4	11
6	. *IEEE Transactions on Signal Processing*, **1994**, 42, 1190-1201	4.8	16
5	Scheduling synchronous dataflow graphs for efficient looping. *Journal of Signal Processing Systems*, **1993**, 6, 271-288		22
4	. *IEEE Transactions on Acoustics, Speech, and Signal Processing*, **1989**, 37, 1751-1762		51

3	Embedded Multiprocessors		67
2	Memory Management for Synthesis of DSP Software		15
1	Learning Compact DNN Models for Behavior Prediction from Neural Activity of Calcium Imaging. *Journal of Signal Processing Systems*,1	1.4	0