

Shuvra S Bhattacharyya

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218
papers

1,865
citations

20
h-index

34
g-index

265
ext. papers

2,257
ext. citations

2.5
avg, IF

4.92
L-index

#	Paper	IF	Citations
218	Parameterized dataflow modeling for DSP systems. <i>IEEE Transactions on Signal Processing</i> , 2001 , 49, 2408-2421	4.8	170
217	Synthesis of Embedded Software from Synchronous Dataflow Specifications. <i>Journal of Signal Processing Systems</i> , 1999 , 21, 151-166		109
216	Hyperspectral Image Classification With Attention-Aided CNNs. <i>IEEE Transactions on Geoscience and Remote Sensing</i> , 2021 , 59, 2281-2293	8.1	89
215	Embedded Multiprocessors		67
214	Functional DIF for Rapid Prototyping 2008 ,		54
213	Systematic integration of parameterized local search into evolutionary algorithms. <i>IEEE Transactions on Evolutionary Computation</i> , 2004 , 8, 137-155	15.6	52
212	Overview of the MPEG Reconfigurable Video Coding Framework. <i>Journal of Signal Processing Systems</i> , 2011 , 63, 251-263	1.4	51
211	. <i>IEEE Transactions on Acoustics, Speech, and Signal Processing</i> , 1989 , 37, 1751-1762		51
210	Software synthesis from the dataflow interchange format 2005 ,		45
209	OpenDF. <i>Computer Architecture News</i> , 2008 , 36, 29-35		43
208	PiMM: Parameterized and Interfaced dataflow Meta-Model for MPSoCs runtime reconfiguration 2013 ,		39
207	Efficient techniques for clustering and scheduling onto embedded multiprocessors. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2006 , 17, 667-680	3.7	33
206	Intermediate Representations for Design Automation of Multiprocessor DSP Systems. <i>Design Automation for Embedded Systems</i> , 2002 , 7, 307-323	0.6	33
205	Joint Minimization of Code and Data for Synchronous Dataflow Programs. <i>Formal Methods in System Design</i> , 1997 , 11, 41-70	1.4	31
204	A generalized static data flow clustering algorithm for mpsoC scheduling of multimedia applications 2008 ,		28
203	Buffer merging – powerful technique for reducing memory requirements of synchronous dataflow specifications. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2004 , 9, 212-237	1.5	26
202	APGAN and RPMC: Complementary Heuristics for Translating DSP Block Diagrams into Efficient Software Implementations. <i>Design Automation for Embedded Systems</i> , 1997 , 2, 33-60	0.6	24

201	Parameterized Looped Schedules for Compact Representation of Execution Sequences in DSP Hardware and Software Implementation. <i>IEEE Transactions on Signal Processing</i> , 2007 , 55, 3126-3138	4.8	23
200	Scheduling synchronous dataflow graphs for efficient looping. <i>Journal of Signal Processing Systems</i> , 1993 , 6, 271-288		22
199	A generalized scheduling approach for dynamic dataflow applications 2009 ,		21
198	Interface-based hierarchy for synchronous data-flow graphs 2009 ,		19
197	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2000 , 8, 452-455	2.6	18
196	Exploiting statically schedulable regions in dataflow programs 2009 ,		17
195	. <i>IEEE Transactions on Signal Processing</i> , 1994 , 42, 1190-1201	4.8	16
194	Exploiting Statically Schedulable Regions in Dataflow Programs. <i>Journal of Signal Processing Systems</i> , 2011 , 63, 129-142	1.4	15
193	Memory Management for Synthesis of DSP Software		15
192	Heterogeneous Design in Functional DIF. <i>Lecture Notes in Computer Science</i> , 2008 , 157-166	0.9	14
191	Design and implementation of embedded computer vision systems based on particle filters. <i>Computer Vision and Image Understanding</i> , 2010 , 114, 1203-1214	4.3	13
190	Joint application mapping/interconnect synthesis techniques for embedded chip-scale multiprocessors. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2005 , 16, 99-112	3.7	13
189	Dynamic Dataflow Graphs 2013 , 905-944		13
188	2013 ,		12
187	Exploring the Concurrency of an MPEG RVC Decoder Based on Dataflow Program Analysis. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , 2009 , 19, 1646-1657	6.4	12
186	. <i>IEEE Transactions on Signal Processing</i> , 1997 , 45, 1605-1618	4.8	12
185	Efficient simulation of critical synchronous dataflow graphs 2006 ,		12
184	Looped schedules for dataflow descriptions of multirate signal processing algorithms. <i>Formal Methods in System Design</i> , 1994 , 5, 183-205	1.4	11

183	Parameterized Sets of Dataflow Modes And Their Application to Implementation of Cognitive Radio Systems. <i>Journal of Signal Processing Systems</i> , 2015 , 80, 3-18	1.4	10
182	Reproducible Evaluation of System Efficiency With a Model of Architecture: From Theory to Practice. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 2050-2063	2.5	10
181	Integration of Dataflow-Based Heterogeneous Multiprocessor Scheduling Techniques in GNU Radio. <i>Journal of Signal Processing Systems</i> , 2013 , 70, 177-191	1.4	10
180	Model-based mapping of reconfigurable image registration on FPGA platforms. <i>Journal of Real-Time Image Processing</i> , 2008 , 3, 149-162	1.9	10
179	2007 ,		10
178	An integrated hardware/software design methodology for signal processing systems. <i>Journal of Systems Architecture</i> , 2019 , 93, 1-19	5.5	10
177	Dynamic, data-driven processing of multispectral video streams. <i>IEEE Aerospace and Electronic Systems Magazine</i> , 2017 , 32, 50-57	2.4	9
176	Analysis of SystemC actor networks for efficient synthesis. <i>Transactions on Embedded Computing Systems</i> , 2010 , 10, 1-34	1.8	9
175	FPGA-based design and implementation of the 3GPP-LTE physical layer using parameterized synchronous dataflow techniques 2010 ,		9
174	Signal processing on platforms with multiple cores: Part 1 - Overview and methodologies [From the Guest Editors]. <i>IEEE Signal Processing Magazine</i> , 2009 , 26, 24-25	9.4	9
173	Multidimensional Exploration of Software Implementations for DSP Algorithms. <i>Journal of Signal Processing Systems</i> , 2000 , 24, 83-98		9
172	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems 2017 , 1185-1219		9
171	Mapping Parameterized Cyclo-static Dataflow Graphs onto Configurable Hardware. <i>Journal of Signal Processing Systems</i> , 2012 , 66, 285-301	1.4	8
170	A Model-Based Schedule Representation for Heterogeneous Mapping of Dataflow Graphs 2011 ,		8
169	Memory-constrained Block Processing for DSP Software Optimization. <i>Journal of Signal Processing Systems</i> , 2008 , 50, 163-177	1.4	8
168	Efficient simulation of critical synchronous dataflow graphs. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2007 , 12, 1-28	1.5	8
167	Energy-Aware Data Compression for Wireless Sensor Networks 2007 ,		8
166	Modeling of Block-Based DSP Systems. <i>Journal of Signal Processing Systems</i> , 2005 , 40, 289-299		8

165	DIF: An Interchange Format for Dataflow-Based Design Tools. <i>Lecture Notes in Computer Science</i> , 2004 , 423-432	0.9	8
164	An accumulative fusion architecture for discriminating people and vehicles using acoustic and seismic signals 2017 ,		7
163	Low-Complexity Digital Predistortion for Reducing Power Amplifier Spurious Emissions in Spectrally-Agile Flexible Radio 2014 ,		7
162	Energy-driven distribution of signal processing applications across wireless sensor networks. <i>ACM Transactions on Sensor Networks</i> , 2010 , 6, 1-32	2.9	7
161	Mode grouping for more effective generalized scheduling of dynamic dataflow applications 2009 ,		7
160	Resource-efficient acceleration of 2-dimensional Fast Fourier Transform computations on FPGAs 2009 ,		7
159	Applying graphics processor acceleration in a software defined radio prototyping environment 2011 ,		7
158	Parameterized design framework for hardware implementation of particle filters. <i>Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing</i> , 2008 ,	1.6	7
157	Affine Nested Loop Programs and their Binary Parameterized Dataflow Graph Counterparts 2006 ,		7
156	PRUNE: Dynamic and Decidable Dataflow for Signal Processing on Heterogeneous Platforms. <i>IEEE Transactions on Signal Processing</i> , 2018 , 66, 654-665	4.8	7
155	Online learning in neural decoding using incremental linear discriminant analysis 2017 ,		6
154	Low power implementation of digital predistortion filter on a heterogeneous application specific multiprocessor 2014 ,		6
153	Efficient architecture mapping of FFT/IFFT for cognitive radio networks 2014 ,		6
152	. <i>IEEE Transactions on Multimedia</i> , 2012 , 14, 630-640	6.6	6
151	Towards systematic exploration of tradeoffs for medical image registration on heterogeneous platforms 2008 ,		6
150	Towards a Heterogeneous Medical Image Registration Acceleration Platform 2007 ,		6
149	Contention-conscious transaction ordering in multiprocessor DSP systems. <i>IEEE Transactions on Signal Processing</i> , 2006 , 54, 556-569	4.8	6
148	Compact Procedural Implementation in DSP Software Synthesis Through Recursive Graph Decomposition. <i>Lecture Notes in Computer Science</i> , 2004 , 47-61	0.9	6

147	Implementation, Scheduling, and Adaptation of Partial Expansion Graphs on Multicore Platforms. <i>Journal of Signal Processing Systems</i> , 2017 , 87, 107-125	1.4	5
146	Multi-Scale Gradient Image Super-Resolution for Preserving SIFT Key Points in Low-Resolution Images. <i>Signal Processing: Image Communication</i> , 2019 , 78, 236-245	2.8	5
145	Model Based Design Environment for Data-driven Embedded Signal Processing Systems ¹ . <i>Procedia Computer Science</i> , 2014 , 29, 1193-1202	1.6	5
144	A Hybrid Task Graph Scheduler for High Performance Image Processing Workflows. <i>Journal of Signal Processing Systems</i> , 2017 , 89, 457-467	1.4	5
143	A hybrid task graph scheduler for high performance image processing workflows 2015 ,		5
142	Implementation of a high-throughput low-latency polyphase channelizer on GPUs. <i>Eurasip Journal on Advances in Signal Processing</i> , 2014 , 2014,	1.9	5
141	Implementation of a low-complexity low-latency arbitrary resampler on GPUs 2014 ,		5
140	Partial Expansion Graphs: Exposing Parallelism and Dynamic Scheduling Opportunities for DSP Applications 2012 ,		5
139	Pipelined FFT for wireless communications supporting 128 ² 048 / 1536 -point transforms 2013 ,		5
138	Scalable representation of dataflow graph structures using topological patterns 2010 ,		5
137	Multithreaded simulation for synchronous dataflow graphs 2008 ,		5
136	Model-Based Mapping of Image Registration Applications onto Configurable Hardware 2006 ,		5
135	A taxonomy for medical image registration acceleration techniques 2007 ,		5
134	Dataflow-Based Mapping of Computer Vision Algorithms onto FPGAs. <i>Eurasip Journal on Embedded Systems</i> , 2007 , 2007, 1-12	2	5
133	Dataflow Transformations in High-level DSP System Design 2006 ,		5
132	Reconfigurable image registration on FPGA platforms 2006 ,		5
131	Adaptive negative cycle detection in dynamic graphs 2001 ,		5
130	Compact modeling and management of reconfiguration in digital channelizer implementation 2016 ,		5

129	Resource-constrained implementation and optimization of a deep neural network for vehicle classification 2016 ,		5
128	Elastic Neural Networks: A Scalable Framework for Embedded Computer Vision 2018 ,		5
127	Efficient Solving of Markov Decision Processes on GPUs Using Parallelized Sparse Matrices 2018 ,		5
126	Energy-Driven Partitioning of Signal Processing Algorithms in Sensor Networks. <i>Lecture Notes in Computer Science</i> , 2006 , 142-154	0.9	5
125	Constant-rate clock recovery and jitter measurement on deep memory waveforms using dataflow 2015 ,		4
124	Prinet: A Prior Driven Spectral Super-Resolution Network 2020 ,		4
123	A novel framework for design and implementation of adaptive stream mining systems 2013 ,		4
122	Hardware design methodology using lightweight dataflow and its integration with low power techniques. <i>Journal of Systems Architecture</i> , 2017 , 78, 15-29	5.5	4
121	Multiobjective Design Optimization in the Lightweight Dataflow for DDDAS Environment (LiD4E) 1. <i>Procedia Computer Science</i> , 2015 , 51, 2563-2572	1.6	4
120	Just-in-time scheduling techniques for multicore signal processing systems 2014 ,		4
119	Topological Patterns for Scalable Representation and Analysis of Dataflow Graphs. <i>Journal of Signal Processing Systems</i> , 2011 , 65, 229-244	1.4	4
118	. <i>IEEE Signal Processing Magazine</i> , 2010 , 27, 20-21	9.4	4
117	Vectorization and mapping of software defined radio applications on heterogeneous multi-processor platforms 2011 ,		4
116	High-Performance Buffer Mapping to Exploit DRAM Concurrency in Multiprocessor DSP Systems 2009 ,		4
115	An architectural level design methodology for smart camera applications. <i>International Journal of Embedded Systems</i> , 2009 , 4, 83	0.5	4
114	Multiobjective Optimization of FPGA-Based Medical Image Registration 2008 ,		4
113	Systematic generation of FPGA-based FFT implementations. <i>Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing</i> , 2008 ,	1.6	4
112	Design and optimization of a distributed, embedded speech recognition system. <i>Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on</i> , 2008 ,		4

111	The pipeline decomposition tree: 2006,		4
110	Low-Overhead Run-Time Scheduling for Fine-Grained Acceleration of Signal Processing Systems. <i>Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007,</i>		4
109	Beyond single-appearance schedules. <i>Transactions on Embedded Computing Systems, 2007, 6, 14</i>	1.8	4
108	A Communication Interface for Multiprocessor Signal Processing Systems 2006,		4
107	. <i>IEEE Transactions on Signal Processing, 2004, 52, 1209-1217</i>	4.8	4
106	Memory-Constrained Vectorization and Scheduling of Dataflow Graphs for Hybrid CPU-GPU Platforms. <i>Transactions on Embedded Computing Systems, 2018, 17, 1-25</i>	1.8	4
105	Models of Architecture: Reproducible Efficiency Evaluation for Signal Processing Systems 2016,		4
104	Weakly supervised segmentation for real-time surgical tool tracking. <i>Healthcare Technology Letters, 2019, 6, 231-236</i>	1.9	4
103	Model-based cosimulation for industrial wireless networks 2018,		4
102	Gradient Image Super-resolution for Low-resolution Image Recognition 2019,		3
101	Reconfigurable Digital Channelizer Design Using Factored Markov Decision Processes. <i>Journal of Signal Processing Systems, 2018, 90, 1329-1343</i>	1.4	3
100	A Wideband Front-End Receiver Implementation on GPUs. <i>IEEE Transactions on Signal Processing, 2016, 64, 2602-2612</i>	4.8	3
99	An optimized embedded target detection system using acoustic and seismic sensors 2017,		3
98	Efficient static buffering to guarantee throughput-optimal FPGA implementation of synchronous dataflow graphs 2010,		3
97	Advances in hardware design and implementation of signal processing systems [DSP Forum]. <i>IEEE Signal Processing Magazine, 2008, 25, 175-180</i>	9.4	3
96	Sensor Support Systems for Asymmetric Threat Countermeasures. <i>IEEE Sensors Journal, 2008, 8, 682-692</i>		3
95	2006,		3
94	Memory-constrained Block Processing Optimization for Synthesis of DSP Software 2006,		3

93	Analysis of Dataflow Programs with Interval-limited Data-rates. <i>Journal of Signal Processing Systems</i> , 2006 , 43, 247-258		3
92	DSP address optimization using evolutionary algorithms 2005 ,		3
91	Segmentation of surgical instruments in laparoscopic videos: training dataset generation and deep-learning-based framework 2019 ,		3
90	Design Methodology for Embedded Computer Vision Systems 2009 , 27-47		3
89	The DSPCAD Integrative Command Line Environment: Introduction to DICE Version 1.1 2011 ,		3
88	Dynamic Dataflow Graphs 2019 , 1173-1210		3
87	The DSPCAD Framework for Modeling and Synthesis of Signal Processing Systems 2016 , 1-35		3
86	Dynamic and Multidimensional Dataflow Graphs 2010 , 899-930		3
85	Heterogeneous Design in Functional DIF. <i>Lecture Notes in Computer Science</i> , 2011 , 391-408	0.9	3
84	A Design Framework for Mapping Vectorized Synchronous Dataflow Graphs onto CPU-GPU Platforms 2016 ,		3
83	Real-Time Calcium Imaging Based Neural Decoding with a Support Vector Machine 2019 ,		3
82	A novel view synthesis approach based on view space covering for gait recognition. <i>Neurocomputing</i> , 2021 , 453, 13-25	5.4	3
81	Evolutionary Multiobjective Optimization for Digital Predistortion Architectures. <i>Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering</i> , 2016 , 498-510 ^{0.2}		2
80	Multi-Frame Super Resolution with Deep Residual Learning on Flow Registered Non-Integer Pixel Images 2019 ,		2
79	Scheduling of parallelized synchronous dataflow actors 2013 ,		2
78	Model-based dynamic scheduling for multicore implementation of image processing systems 2017 ,		2
77	Model-based design and implementation of an adaptive digital predistortion filter 2015 ,		2
76	High-performance and low-energy buffer mapping method for multiprocessor DSP systems. <i>Transactions on Embedded Computing Systems</i> , 2013 , 12, 1-23	1.8	2

75	Simulating dynamic communication systems using the core functional dataflow model 2010 ,		2
74	. <i>IEEE Signal Processing Magazine</i> , 2010 , 27, 61-68	9.4	2
73	Loop transformations for interface-based hierarchies IN SDF graphs 2010 ,		2
72	Dataflow-based implementation of model predictive control 2009 ,		2
71	Design methods for Wireless Sensor Network Building Energy Monitoring Systems 2011 ,		2
70	Multithreaded Simulation for Synchronous Dataflow Graphs. <i>ACM Transactions on Design Automation of Electronic Systems</i> , 2011 , 16, 1-23	1.5	2
69	Parameterized scheduling for signal processing systems using topological patterns 2012 ,		2
68	A Low-overhead Scheduling Methodology for Fine-grained Acceleration of Signal Processing Systems. <i>Journal of Signal Processing Systems</i> , 2010 , 60, 333-343	1.4	2
67	Multiobjective Optimization for Reconfigurable Implementation of Medical Image Registration. <i>International Journal of Reconfigurable Computing</i> , 2008 , 2008, 1-17	2.1	2
66	Configuration and Representation of Large-Scale Dataflow Graphs using the Dataflow Interchange Format. <i>Signal Processing Systems Design and Implementation (siPS)</i> , <i>IEEE Workshop on</i> , 2006 ,		2
65	Logic Foundry: Rapid Prototyping for FPGA-Based DSP Systems. <i>Eurasip Journal on Advances in Signal Processing</i> , 2003 , 2003, 1	1.9	2
64	Shared memory implementations of synchronous dataflow specifications 2000 ,		2
63	Instrumentation-Driven Model Detection and Actor Partitioning for Dataflow Graphs. <i>International Journal of Embedded and Real-Time Communication Systems</i> , 2013 , 4, 1-21	0.6	2
62	Scheduling of Synchronous Dataflow Graphs with Partially Periodic Real-Time Constraints 2020 ,		2
61	Data-Driven Stream Mining Systems for Computer Vision. <i>Advances in Computer Vision and Pattern Recognition</i> , 2014 , 249-264	1.1	2
60	. <i>Computer</i> , 2020 , 53, 71-75	1.6	2
59	MADS: A Framework for Design and Implementation of Adaptive Digital Predistortion Systems. <i>IEEE Journal on Emerging and Selected Topics in Circuits and Systems</i> , 2019 , 9, 712-722	5.2	2
58	Generalized Graph Connections for Dataflow Modeling of DSP Applications 2018 ,		2

57	PathTracing: Raising the Level of Understanding of Processing Latency in Heterogeneous MPSoCs 2021 ,		2
56	Data Flow Algorithms for Processors with Vector Extensions. <i>Journal of Signal Processing Systems</i> , 2017 , 87, 21-31	1.4	1
55	Decidable Variable-Rate Dataflow for Heterogeneous Signal Processing Systems 2020 ,		1
54	Real-Time Neuron Detection and Neural Signal Extraction Platform for Miniature Calcium Imaging. <i>Frontiers in Computational Neuroscience</i> , 2020 , 14, 43	3.5	1
53	A design tool for high performance image processing on multicore platforms 2018 ,		1
52	Jitter measurement on deep waveforms with constant memory 2016 ,		1
51	Model-Based Representations for Dataflow Schedules. <i>Lecture Notes in Computer Science</i> , 2018 , 88-105	0.9	1
50	Design Space Exploration for Wireless-Integrated Factory Automation Systems 2019 ,		1
49	Optimized implementation of digital signal processing applications with gapless data acquisition. <i>Eurasip Journal on Advances in Signal Processing</i> , 2019 , 2019,	1.9	1
48	Mapping Parameterized Dataflow Graphs onto FPGA Platforms. <i>Academic Press Library in Signal Processing</i> , 2014 , 4, 643-673		1
47	Instrumentation-driven framework for validation of dataflow applications 2014 ,		1
46	Parameterized Scheduling of Topological Patterns in Signal Processing Dataflow Graphs. <i>Journal of Signal Processing Systems</i> , 2013 , 71, 275-286	1.4	1
45	A Design Methodology for Distributed Adaptive Stream Mining Systems. <i>Procedia Computer Science</i> , 2013 , 18, 2482-2491	1.6	1
44	Low-power heterogeneous computing via adaptive execution of dataflow actors 2017 ,		1
43	An efficient GPU implementation of a multirate resampler for multi-carrier systems 2015 ,		1
42	Data flow algorithms for processors with vector extensions: Handling actors with internal state 2014 ,		1
41	Partial expansion of dataflow graphs for resource-aware scheduling of multicore signal processing systems 2014 ,		1
40	Dynamic, data-driven spectrum management in cognitive small cell networks 2014 ,		1

39	Multidimensional Dataflow Graph Modeling and Mapping for Efficient GPU Implementation 2012 ,		1
38	Configurable, resource-optimized FFT architecture for OFDM communication 2013 ,		1
37	Automated generation of an efficient MPEG-4 Reconfigurable Video Coding decoder implementation 2010 ,		1
36	Rapid prototyping for digital signal processing systems using Parameterized Synchronous Dataflow graphs 2010 ,		1
35	Improving the performance of active set based Model Predictive Controls by dataflow methods 2009 ,		1
34	Integration of Dataflow optimization techniques into a software radio design framework 2009 ,		1
33	An Optimized Message Passing Framework for Parallel Implementation of Signal Processing Applications 2008 ,		1
32	Compact, Low Power Wireless Sensor Network System for Line Crossing Recognition 2007 ,		1
31	Register File Partitioning with Constraint Programming 2006 ,		1
30	The CBP Parameter: A Module Characterization Approach for DSP Software Optimization. <i>Journal of Signal Processing Systems</i> , 2004 , 38, 131-146		1
29	Design of a Dynamic Data-Driven System for Multispectral Video Processing 2018 , 529-545		1
28	Runtime Adaptation in Wireless Sensor Nodes Using Structured Learning. <i>ACM Transactions on Cyber-Physical Systems</i> , 2020 , 4, 1-28	2.3	1
27	Hyperspectral Video Processing on Resource-Constrained Platforms 2019 ,		1
26	Dataflow-Based, Cross-Platform Design Flow for DSP Applications. <i>Embedded Systems</i> , 2014 , 41-65		1
25	Implementation of a Multirate Resampler for Multi-carrier Systems on GPUs. <i>Journal of Signal Processing Systems</i> , 2017 , 89, 445-455	1.4	0
24	Introduction to Hardware/Software Codesign 2017 , 3-26		0
23	Scheduling of Parallelized Synchronous Dataflow Actors for Multicore Signal Processing. <i>Journal of Signal Processing Systems</i> , 2016 , 83, 309-328	1.4	0
22	Neural decoding on imbalanced calcium imaging data with a network of support vector machines. <i>Advanced Robotics</i> , 2021 , 35, 459-470	1.7	0

21	Dynamic, Data-Driven Hyperspectral Image Classification on Resource-Constrained Platforms. <i>Lecture Notes in Computer Science</i> , 2020 , 320-327	0.9	0
20	Learning Compact DNN Models for Behavior Prediction from Neural Activity of Calcium Imaging. <i>Journal of Signal Processing Systems</i> , 1	1.4	0
19	CGMBE: a model-based tool for the design and implementation of real-time image processing applications on CPU/GPU platforms. <i>Journal of Real-Time Image Processing</i> , 2021 , 18, 561-583	1.9	0
18	Software synthesis from dataflow schedule graphs. <i>SN Applied Sciences</i> , 2021 , 3, 1	1.8	0
17	Instrumentation-Driven Validation of Dataflow Applications. <i>Journal of Signal Processing Systems</i> , 2016 , 84, 383-397	1.4	
16	Introduction to the Special Issue on Embedded Computing Systems for DSP. <i>Journal of Signal Processing Systems</i> , 2008 , 50, 97-98	1.4	
15	High-Level Synthesis of DSP Applications Using Adaptive Negative Cycle Detection. <i>Eurasip Journal on Advances in Signal Processing</i> , 2002 , 2002, 1	1.9	
14	Spectral Super Resolution with DCT Decomposition and Deep Residual Learning. <i>Lecture Notes in Computer Science</i> , 2020 , 171-178	0.9	
13	Rapid Quality Assessment of Nonrigid Image Registration Based on Supervised Learning. <i>Journal of Digital Imaging</i> , 2021 , 34, 1376	5.3	
12	Generating Compact Code from Dataflow Specifications of Multirate Signal Processing Algorithms 2002 , 452-464		
11	Dynamic Data Driven Application Systems (DDDAS) for Multimedia Content Analysis 2018 , 631-651		
10	GEMBench: A Platform for Collaborative Development of GPU Accelerated Embedded Markov Decision Systems. <i>Lecture Notes in Computer Science</i> , 2019 , 294-308	0.9	
9	Passive-Active Flowgraphs for Efficient Modeling and Design of Signal Processing Systems. <i>Journal of Signal Processing Systems</i> , 2020 , 92, 1133-1151	1.4	
8	Model-Based Dynamic Scheduling for Multicore Signal Processing. <i>Journal of Signal Processing Systems</i> , 2019 , 91, 981-994	1.4	
7	Rotators in Fast Fourier Transforms 2020 , 245-262		
6	WGEVIA: A Graph Level Embedding Method for Microcircuit Data. <i>Frontiers in Computational Neuroscience</i> , 2020 , 14, 603765	3.5	
5	VR-PRUNE: Decidable Variable-Rate Dataflow for Signal Processing Systems. <i>IEEE Transactions on Signal Processing</i> , 2022 , 1-1	4.8	
4	PathTracer: Understanding Response Time of Signal Processing Applications on Heterogeneous MPSoCs. <i>ACM Transactions on Modeling and Performance Evaluation of Computing Systems</i> , 2021 , 6, 1-30	0.8	

- 3 A Framework for Fixed Priority Periodic Scheduling Synthesis from Synchronous Data-Flow Graphs. *Lecture Notes in Computer Science*, **2022**, 259-271 0.9
- 2 Multimedia Content Analysis with Dynamic Data Driven Applications Systems (DDDAS) **2022**, 645-667
- 1 Design of a Dynamic Data-Driven System for Multispectral Video Processing **2022**, 539-556