Shuyu Bao

List of Publications by Year
in descending order

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29	658	687220 13	794469 19
papers	citations	h-index	g-index

29	29	29	800
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Low-threshold optically pumped lasing in highly strained germanium nanowires. Nature Communications, 2017, 8, 1845.	5.8	131
2	Germanium-on-silicon nitride waveguides for mid-infrared integrated photonics. Applied Physics Letters, 2016, 109, .	1.5	66
3	High-efficiency normal-incidence vertical p-i-n photodetectors on a germanium-on-insulator platform. Photonics Research, 2017, 5, 702.	3.4	52
4	Fabrication and characterization of germanium-on-insulator through epitaxy, bonding, and layer transfer. Journal of Applied Physics, 2014, 116, .	1.1	49
5	Reduction of threading dislocation density in Ge/Si using a heavily As-doped Ge seed layer. AIP Advances, 2016, 6, .	0.6	47
6	Defects reduction of Ge epitaxial film in a germanium-on-insulator wafer by annealing in oxygen ambient. APL Materials, 2015, 3, .	2.2	43
7	A review of silicon-based wafer bonding processes, an approach to realize the monolithic integration of Si-CMOS and IIIâ€“V-on-Si wafers. Journal of Semiconductors, 2021, 42, 023106.	2.0	34
8	Integration of GaAs, GaN, and Si-CMOS on a common 200 mm Si substrate through multilayer transfer process. Applied Physics Express, 2016, 9, 086501.	1.1	33
9	GeSn-on-insulator substrate formed by direct wafer bonding. Applied Physics Letters, 2016, 109, .	1.5	31
10	The role of AsH3 partial pressure on anti-phase boundary in GaAs-on-Ge grown by MOCVD â€“ Application to a 200mm GaAs virtual substrate. Journal of Crystal Growth, 2015, 421, 58-65.	0.7	28
11	Integration of IIIâ€“V materials and Si-CMOS through double layer transfer process. Japanese Journal of Applied Physics, 2015, 54, 030209.	0.8	21
12	Monolithic Integration of Si-CMOS and III-V-on-Si Through Direct Wafer Bonding Process. IEEE Journal of the Electron Devices Society, 2018, 6, 571-578.	1.2	19
13	The first GeSn FinFET on a novel GeSnOI substrate achieving lowest S of 79 mV/decade and record high Gm, int of 807 Î¼S/Î¼m for GeSn P-FETs. , 2017, , .		18
14	Hetero-epitaxy of high quality germanium film on silicon substrate for optoelectronic integrated circuit applications. Journal of Materials Research, 2017, 32, 4025-4040.	1.2	15
15	Monolithic integration of IIIâ€“V HEMT and Si-CMOS through TSV-less 3D wafer stacking. , 2015, , .		14
16	Suppression of interfacial voids formation during silane (SiH4)-based silicon oxide bonding with a thin silicon nitride capping layer. Journal of Applied Physics, 2018, 123, .	1.1	14
17	High-performance AlGaInP light-emitting diodes integrated on silicon through a superior quality germanium-on-insulator. Photonics Research, 2018, 6, 290.	3.4	8
18	Thermal stability of germanium-tin (GeSn) fins. Applied Physics Letters, 2017, 111, 252103.	1.5	7

#	Article	IF	Citations
19	Ge-on-insulator lateral p-i-n waveguide photodetectors for optical communication. Optics Letters, 2020, 45, 6683.	1.7	7
20	Strain relaxation of germanium-tin (GeSn) fins. AIP Advances, 2018, 8, 025111.	0.6	6
21	Germanium-on-insulator virtual substrate for InGaP epitaxy. Materials Science in Semiconductor Processing, 2017, 58, 15-21.	1.9	5
22	Extension of Germanium-on-insulator optical absorption edge using CMOS-compatible silicon nitride stressor. , 2017, , .		4
23	Systematic Investigation and Characterization of Ag Paste for LED Die Attach. , 2021, , .		4
24	Fabrication of germanium-on-insulator (GOI) with improved threading dislocation density (TDD) via buffer-less epitaxy and bonding. , 2014, , .		2
25	Integration of III–V materials and Si-CMOS through double layer transfer process. , 2014, , .		0
26	Modeling and fabrication of Ge-on-Si<inf>3</inf>N<inf>4</inf> for low bend-loss waveguides. , 2016, , .		0
27	Epitaxy and wafer bonding of AlGaInP multiple-quantum wells and light-emitting diodes on 8â€³ Si substrates. , 2016, , .		0
28	High quality Ge-OI, IIIâ€“V-OI on 200 mm Si substrate. , 2016, , .		0
29	Germanium-on-insulator virtual substrate for InGaP epitaxy. Materials Science in Semiconductor Processing, 2017, 70, 17-23.	1.9	0