Fumito Imura

List of Publications by Year
in descending order

18 papers	128 citations	1937685 4 h-index	1872680 6 g-index
18 all docs	18 docs citations	18 times ranked	112 citing authors

#	Article	IF	Citations
1	Analyses on Cleanroom-Free Performance and Transistor Manufacturing Cycle Time of Minimal Fab. IEEE Transactions on Semiconductor Manufacturing, 2015, 28, 551-556.	1.7	42
2	Development of nano-surgery system for cell organelles. , 0, , .		13
3	Impact of die thinning on the thermal performance of a central TSV bus in a 3D stacked circuit. Microelectronics Journal, 2015, 46, 1106-1113.	2.0	12
4	Functional demonstration of the ability of a primary spermatogonium as a stem cell by tracing a single cell destiny in Xenopus laevis. Development Growth and Differentiation, 2006, 48, 525-535.	1.5	11
5	Development of micro bump joints fabrication process using cone shape Au bumps for 3D LSI chip stacking. , 2014, , .		10
6	COOL interconnect low power interconnection technology for scalable 3D LSI design. , 2011, , .		9
7	Wide bus chip-to-chip interconnection technology using fine pitch bump joint array for 3D LSI chip stacking. , 2012, , .		7
8	Cool System scalable 3-D stacked heterogeneous Multi-Core / Multi-Chip architecture for ultra low-power digital TV applications. , 2012, , .		6
9	Attoliter Control of Microliquid. Japanese Journal of Applied Physics, 2007, 46, 7519.	1.5	4
10	Cool Interconnect: A 1024-bit Wide Bus for Chip-to-Chip Communications in 3-D Integrated Circuits. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2019, 9, 525-535.	2.5	4
11	Investigation of effects of die thinning on central TSV bus driver thermal performance. , 2014, , .		3
12	Method for back-annotating per-transistor power values onto 3DIC layouts to enable detailed thermal analysis. , 2014, , .		3
13	Development of Semiconductor Manufacturing System Integrating Wafer Process and Packaging Process Using a Half-Inch Sized Package. , 2018, , .		2
14	Via Interconnections for Half-Inch Sized Package Fabricated by Minimal Fab. , 2018, , .		1
15	Ultra-Compact Device-Manufacturing-System â€œMinimal Fabâ€•Integrating Wafer and Packaging Process for High-Mix Low-Volume Productions and Its Packaging Applications. Journal of Japan Institute of Electronics Packaging, 2019, 22, 507-513.	0.1	1
16	Work function alternation on Peierls transition of K_{0.3}MoO₃. European Physical Journal Special Topics, 2005, 131, 351-353.	0.2	0
17	BGA packaging process for a device made by minimal fab. , 2017, , .		0
18	Via Interconnections for Half-Inch Packaging of Electronic Devices Using Minimal Fab Process Tools. Journal of Photopolymer Science and Technology = [Fotoporima Konwakai Shi], 2020, 32, 763-768.	0.3	0