

Leibo Liu

List of Publications by Year in Descending Order

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The third column is the impact factor (IF) of the journal, and the fourth column is the number of citations of the article.

253 papers	2,193 citations	22 h-index	37 g-index
340 ext. papers	3,095 ext. citations	2.8 avg, IF	5.37 L-index

#	Paper	IF	Citations
253	BitCluster: Fine-Grained Weight Quantization for Load-Balanced Bit-Serial Neural Network Accelerators. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2022 , 1-1	2.5	
252	Design of Majority Logic-based Approximate Booth Multipliers for Error-Tolerant Applications. <i>IEEE Nanotechnology Magazine</i> , 2022 , 1-1	2.6	1
251	An energy-efficient dynamically reconfigurable cryptographic engine with improved power/EM-side-channel-attack resistance. <i>Science China Information Sciences</i> , 2022 , 65, 1	3.4	
250	SDP: Co-Designing Algorithm, Dataflow, and Architecture for in-SRAM Sparse NN Acceleration. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2022 , 1-1	2.5	
249	An Energy-Efficient Approximate Divider Based on Logarithmic Conversion and Piecewise Constant Approximation. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2022 , 1-14	3.9	
248	Dynamic-II Pipeline: Compiling Loops with Irregular Branches on Static-Scheduling CGRA. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	0
247	A 12.1 TOPS/W Quantized Network Acceleration Processor With Effective-Weight-Based Convolution and Error-Compensation-Based Prediction. <i>IEEE Journal of Solid-State Circuits</i> , 2021 , 1-1	5.5	0
246	LWRpro: An Energy-Efficient Configurable Crypto-Processor for Module-LWR. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2021 , 68, 1146-1159	3.9	7
245	. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2021 , 68, 1217-1230	3.9	7
244	Fast substitution-box evaluation algorithm and its efficient masking scheme for block ciphers. <i>Science China Information Sciences</i> , 2021 , 64, 1	3.4	0
243	A Logarithmic Floating-Point Multiplier for the Efficient Training of Neural Networks 2021 ,		1
242	. <i>IEEE Transactions on Multimedia</i> , 2021 , 23, 1122-1135	6.6	0
241	Evolver: A Deep Learning Processor With On-Device Quantization/Voltage/Frequency Tuning. <i>IEEE Journal of Solid-State Circuits</i> , 2021 , 56, 658-673	5.5	17
240	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 40, 1896-1908	2.5	1
239	Security-Driven Placement and Routing Tools for Electromagnetic Side-Channel Protection. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 40, 1077-1089	2.5	2
238	A Multiple-Precision Multiply and Accumulation Design with Multiply-Add Merged Strategy for AI Accelerating 2021 ,		1
237	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	0

236	An Efficient FHE Radix-2 Addition Algorithm in BGV Scheme. <i>Journal of Physics: Conference Series</i> , 2021 , 1993, 012030	0.3	
235	Jintide: Utilizing Low-Cost Reconfigurable External Monitors to Substantially Enhance Hardware Security of Large-Scale CPU Clusters. <i>IEEE Journal of Solid-State Circuits</i> , 2021 , 56, 2585-2601	5.5	3
234	Erratum to Eolver: a Deep Learning Processor With On-Device Quantization-Voltage-Frequency Tuning[Feb 21 658-673]. <i>IEEE Journal of Solid-State Circuits</i> , 2021 , 56, 2895-2895	5.5	
233	On-Chip Trust Evaluation Utilizing TDC-Based Parameter-Adjustable Security Primitive. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 40, 1985-1994	2.5	3
232	. <i>IEEE Journal of Solid-State Circuits</i> , 2021 , 56, 3021-3038	5.5	1
231	An Elastic Task Scheduling Scheme on Coarse-Grained Reconfigurable Architectures. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2021 , 32, 3066-3080	3.7	0
230	Security Oriented Design Framework for EM Side-Channel Protection in RTL Implementations. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2021 , 1-1	2.5	
229	Architecture, challenges and applications of dynamic reconfigurable computing. <i>Journal of Semiconductors</i> , 2020 , 41, 021401	2.3	1
228	. <i>IEEE Transactions on Signal Processing</i> , 2020 , 68, 573-588	4.8	18
227	Dynamic Frequency Scaling Aware Opportunistic Through-Silicon-Via Inductor Utilization in Resonant Clocking. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 39, 281-293	2.5	3
226	. <i>IEEE Transactions on Wireless Communications</i> , 2020 , 19, 1025-1037	9.6	13
225	Achieving Flexible Global Reconfiguration in NoCs Using Reconfigurable Rings. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2020 , 31, 611-622	3.7	2
224	NTTU: An Area-Efficient Low-Power NTT-Uncoupled Architecture for NTT-Based Multiplication. <i>IEEE Transactions on Computers</i> , 2020 , 69, 520-533	2.5	3
223	A Multi-Task Hardwired Accelerator for Face Detection and Alignment. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , 2020 , 30, 4284-4298	6.4	8
222	. <i>IEEE Journal of Solid-State Circuits</i> , 2020 , 55, 505-519	5.5	5
221	Pattern-Based Dynamic Compilation System for CGRAs With Online Configuration Transformation. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2020 , 31, 2981-2994	3.7	2
220	Aggressive Fine-Grained Power Gating of NoC Buffers. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 39, 3177-3189	2.5	1
219	Approximate Arithmetic Circuits: A Survey, Characterization, and Recent Applications. <i>Proceedings of the IEEE</i> , 2020 , 108, 2108-2135	14.3	39

218	TFE: Energy-efficient Transferred Filter-based Engine to Compress and Accelerate Convolutional Neural Networks 2020 ,		3
217	A Deflection-Based Deadlock Recovery Framework to Achieve High Throughput for Faulty NoCs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2020 , 1-1	2.5	0
216	A 60 Gb/s-Level Coarse-Grained Reconfigurable Cryptographic Processor With Less Than 1-W Power. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2020 , 67, 375-379	3.5	3
215	A Survey of Coarse-Grained Reconfigurable Architecture and Design. <i>ACM Computing Surveys</i> , 2020 , 52, 1-39	13.4	34
214	An Ultra-Low Power Binarized Convolutional Neural Network-Based Speech Recognition Processor With On-Chip Self-Learning. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2019 , 66, 4648-4661	3.9	20
213	Optimal design of a low-power, phase-switching modulator for implantable medical applications. <i>The Integration VLSI Journal</i> , 2019 , 69, 289-300	1.4	1
212	Pj-AxMTJ: Process-in-memory with Joint Magnetization Switching for Approximate Computing in Magnetic Tunnel Junction 2019 ,		2
211	A Fast and Power-Efficient Hardware Architecture for Non-Maximum Suppression. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2019 , 66, 1870-1874	3.5	5
210	A General Pattern-Based Dynamic Compilation Framework for Coarse-Grained Reconfigurable Architectures 2019 ,		8
209	A 1.17 TOPS/W, 150fps Accelerator for Multi-Face Detection and Alignment 2019 ,		4
208	Characterizing Approximate Adders and Multipliers Optimized under Different Design Constraints 2019 ,		10
207	Dynamic Reconfigurable Chips for Massive MIMO Detection 2019 , 229-306		
206	Nonlinear Massive MIMO Signal Detection Algorithm 2019 , 165-203		
205	Architecture for Nonlinear Massive MIMO Detection 2019 , 205-228		
204	Linear Massive MIMO Detection Algorithm 2019 , 71-123		2
203	Architecture of Linear Massive MIMO Detection 2019 , 125-163		
202	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 1265-1277	2.5	1
201	A High-Performance and Energy-Efficient FIR Adaptive Filter Using Approximate Distributed Arithmetic Circuits. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2019 , 66, 313-326	3.9	23

200	A Face Alignment Accelerator Based on Optimized Coarse-to-Fine Shape Searching. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , 2019 , 29, 2467-2481	6.4	3
199	. <i>IEEE Transactions on Multimedia</i> , 2019 , 21, 943-956	6.6	12
198	Parana: A Parallel Neural Architecture Considering Thermal Problem of 3D Stacked Memory. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2019 , 30, 146-160	3.7	3
197	A Lifetime Reliability-Constrained Runtime Mapping for Throughput Optimization in Many-Core Systems. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 1771-1784	2.5	3
196	MSAM: A Multi-Layer Bi-LSTM Based Speech to Vector Model with Residual Attention Mechanism 2019 ,		2
195	2019 ,		20
194	Addition Circuit optimization Using Carry-Lookahead and SIMD for Homomorphic Encryption 2019 ,		2
193	An Energy-Efficient and Noise-Tolerant Recurrent Neural Network Using Stochastic Computing. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2019 , 27, 2213-2221	2.6	18
192	. <i>IEEE Transactions on Computers</i> , 2019 , 68, 1635-1646	2.5	14
191	2019 ,		3
190	An Energy-Efficient Reconfigurable Processor for Binary-and Ternary-Weight Neural Networks With Flexible Data Bit Width. <i>IEEE Journal of Solid-State Circuits</i> , 2019 , 54, 1120-1136	5.5	32
189	Data-Flow Graph Mapping Optimization for CGRA With Deep Reinforcement Learning. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 2271-2283	2.5	8
188	Reconfigurable Architecture for Neural Approximation in Multimedia Computing. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , 2019 , 29, 892-906	6.4	3
187	A High Throughput Acceleration for Hybrid Neural Networks With Efficient Resource Management on FPGA. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 678-691	2.5	23
186	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2019 , 38, 208-219	2.5	5
185	Multi-Bank Memory Aware Force Directed Scheduling for High-Level Synthesis. <i>IEEE Access</i> , 2018 , 6, 7526-7540	3.5	1
184	A Fast and Power-Efficient Hardware Architecture for Visual Feature Detection in Affine-SIFT. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2018 , 65, 3362-3375	3.9	2
183	Triggered-Issuance and Triggered-Execution: A Control Paradigm to Minimize Pipeline Stalls in Distributed Controlled Coarse-Grained Reconfigurable Arrays. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2018 , 29, 2360-2372	3.7	

182	Stress-Aware Loops Mapping on CGRAs with Dynamic Multi-Map Reconfiguration. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2018 , 29, 2105-2120	3.7	3
181	Anole: A Highly Efficient Dynamically Reconfigurable Crypto-Processor for Symmetric-Key Algorithms. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 3081-3094 ³	3.5	3
180	. <i>IEEE Transactions on Circuits and Systems I: Regular Papers</i> , 2018 , 65, 1717-1730	3.9	23
179	Algorithm and Architecture of a Low-Complexity and High-Parallelism Preprocessing-Based K-Best Detector for Large-Scale MIMO Systems. <i>IEEE Transactions on Signal Processing</i> , 2018 , 66, 1860-1875	4.8	21
178	A High Energy Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications. <i>IEEE Journal of Solid-State Circuits</i> , 2018 , 53, 968-982	5.5	101
177	Memory Partitioning for Parallel Multipattern Data Access in Multiple Data Arrays. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 431-444	2.5	2
176	HReA: An Energy-Efficient Embedded Dynamically Reconfigurable Fabric for 13-Dwarfs Processing. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2018 , 65, 381-385	3.5	14
175	FP-BNN: Binarized neural network on FPGA. <i>Neurocomputing</i> , 2018 , 275, 1072-1086	5.4	138
174	LCP 2018 ,		7
173	RANA: Towards Efficient Neural Acceleration with Refresh-Optimized Embedded DRAM 2018 ,		27
172	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 2519-2529	2.5	21
171	2018 ,		11
170	Bit-width Adaptive Accelerator Design for Convolution Neural Network 2018 ,		3
169	CDPM: Context-Directed Pattern Matching Prefetching to Improve Coarse-Grained Reconfigurable Array Performance. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 1171-1184	2.5	2
168	Bit-Level Disturbance-Aware Memory Partitioning for Parallel Data Access for MLC STT-RAM. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2018 , 26, 2345-2357	2.6	1
167	Physical Attack Countermeasures for Reconfigurable Cryptographic Processors 2018 , 253-333		
166	Compilation Method of Reconfigurable Cryptographic Processors 2018 , 169-211		
165	Examples of Reconfigurable Cryptographic Processor Design 2018 , 213-251		

164	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 782-795	2.5	5
163	A 141 UW, 2.46 PJ/Neuron Binarized Convolutional Neural Network Based Self-Learning Speech Recognition Processor in 28NM CMOS 2018 ,		24
162	Area-Efficient Delay-based PUF Based on Logic Gates 2018 ,		2
161	An Ultra-High Energy-Efficient Reconfigurable Processor for Deep Neural Networks with Binary/Ternary Weights in 28NM CMOS 2018 ,		7
160	Gradient Descent Using Stochastic Circuits for Efficient Training of Learning Machines. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2018 , 37, 2530-2541	2.5	13
159	Stochastic Analysis of Multiplex Boolean Networks for Understanding Epidemic Propagation. <i>IEEE Access</i> , 2018 , 6, 35292-35304	3.5	18
158	Breaking the Synchronization Bottleneck with Reconfigurable Transactional Execution. <i>IEEE Computer Architecture Letters</i> , 2018 , 17, 147-150	1.8	
157	An AdaBoost-Based Face Detection System Using Parallel Configurable Architecture With Optimized Computation. <i>IEEE Systems Journal</i> , 2017 , 11, 260-271	4.3	11
156	CIACP: A Correlation- and Iteration- Aware Cache Partitioning Mechanism to Improve Performance of Multiple Coarse-Grained Reconfigurable Arrays. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2017 , 28, 29-43	3.7	9
155	Energy-aware loops mapping on multi-vdd CGRAs without performance degradation 2017 ,		4
154	Deep Convolutional Neural Network Architecture With Reconfigurable Computation Patterns. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2017 , 25, 2220-2233	2.6	132
153	Low-Computing-Load, High-Parallelism Detection Method Based on Chebyshev Iteration for Massive MIMO Systems With VLSI Architecture. <i>IEEE Transactions on Signal Processing</i> , 2017 , 65, 3775-3788	4.8	18
152	Conflict-Free Loop Mapping for Coarse-Grained Reconfigurable Architecture with Multi-Bank Memory. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2017 , 28, 2471-2485	3.7	8
151	DFGNet: Mapping dataflow graph onto CGRA by a deep learning approach 2017 ,		6
150	Hardware efficient signal detector based on lanczos method for massive MIMO systems 2017 ,		2
149	Aggressive Pipelining of Irregular Applications on Reconfigurable Hardware 2017 ,		9
148	A Review, Classification, and Comparative Evaluation of Approximate Arithmetic Circuits. <i>ACM Journal on Emerging Technologies in Computing Systems</i> , 2017 , 13, 1-34	1.7	104
147	A 1.06-to-5.09 TOPS/W reconfigurable hybrid-neural-network processor for deep learning applications 2017 ,		37

146	Bit-Width Based Resource Partitioning for CNN Acceleration on FPGA 2017 ,		11
145	A 700fps Optimized Coarse-to-Fine Shape Searching Based Hardware Accelerator for Face Alignment 2017 ,		2
144	PMCC: Fast and Accurate System-Level Power Modeling for Processors on Heterogeneous SoC. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2017 , 64, 540-544	3.5	1
143	Exploration of Benes Network in Cryptographic Processors: A Random Infection Countermeasure for Block Ciphers Against Fault Attacks. <i>IEEE Transactions on Information Forensics and Security</i> , 2017 , 12, 309-322	8	16
142	A Multi-Objective Model Oriented Mapping Approach for NoC-based Computing Systems. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2017 , 28, 662-676	3.7	17
141	Reconfigurable VLSI Architecture for Real-Time 2D-to-3D Conversion. <i>IEEE Access</i> , 2017 , 5, 26604-26613	3.5	1
140	Memory partitioning-based modulo scheduling for high-level synthesis 2017 ,		1
139	An efficient hardware design for cerebellar models using approximate circuits 2017 ,		1
138	AEPE: An area and power efficient RRAM crossbar-based accelerator for deep CNNs 2017 ,		9
137	Implementation of in-loop filter for HEVC decoder on reconfigurable processor. <i>IET Image Processing</i> , 2017 , 11, 685-692	1.7	2
136	Multi-CNN and decision tree based driving behavior evaluation 2017 ,		4
135	Aggressive Pipelining of Irregular Applications on Reconfigurable Hardware. <i>Computer Architecture News</i> , 2017 , 45, 575-586		5
134	Learning Convolutional Neural Networks for Data-Flow Graph Mapping on Spatial Programmable Architectures (Abstract Only) 2017 ,		3
133	TLIA: Efficient Reconfigurable Architecture for Control-Intensive Kernels with Triggered-Long-Instructions. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2016 , 27, 2143-2154	3.7	6
132	A 135-frames/s 1080p 87.5-mW Binary-Descriptor-Based Image Feature Extraction Accelerator. <i>IEEE Transactions on Circuits and Systems for Video Technology</i> , 2016 , 26, 1532-1543	6.4	7
131	A Configurable Parallel Hardware Architecture for Efficient Integral Histogram Image Computing. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 1305-1318	2.6	2
130	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 507-520	2.6	6
129	Reliability Evaluation of Phased-Mission Systems Using Stochastic Computation. <i>IEEE Transactions on Reliability</i> , 2016 , 65, 1612-1623	4.6	16

128	Multibank memory optimization for parallel data access in multiple data arrays 2016 ,		10
127	Large-scale MIMO detection design and FPGA implementations using SOR method 2016 ,		16
126	Data cache prefetching via context directed pattern matching for coarse-grained reconfigurable arrays 2016 ,		6
125	2016 ,		3
124	CWFP: Novel Collective Writeback and Fill Policy for Last-Level DRAM Cache. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 2548-2561	2.6	1
123	. <i>IEEE Transactions on Parallel and Distributed Systems</i> , 2016 , 27, 3199-3213	3.7	8
122	Joint Modulo Scheduling and V_{dd} Assignment for Loop Mapping on Dual- V_{dd} CGRAs. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2016 , 35, 1475-1488	2.5	6
121	Against Double Fault Attacks: Injection Effort Model, Space and Time Randomization Based Countermeasures for Reconfigurable Array Architecture. <i>IEEE Transactions on Information Forensics and Security</i> , 2016 , 11, 1151-1164	8	14
120	A Fast and Power-Efficient Memory-Centric Architecture for Affine Computation. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2016 , 63, 668-672	3.5	
119	A Coarse-Grained Reconfigurable Architecture for Compute-Intensive MapReduce Acceleration. <i>IEEE Computer Architecture Letters</i> , 2016 , 15, 69-72	1.8	5
118	Memory-Aware Loop Mapping on Coarse-Grained Reconfigurable Architectures. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 1895-1908	2.6	22
117	Trigger-Centric Loop Mapping on CGRAs. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2016 , 24, 1998-2002	2.6	5
116	An Implementation of Multiple-Standard Video Decoder on a Mixed-Grained Reconfigurable Computing Platform. <i>IEICE Transactions on Information and Systems</i> , 2016 , E99.D, 1285-1295	0.6	3
115	Joint loop mapping and data placement for coarse-grained reconfigurable architecture with multi-bank memory 2016 ,		4
114	A fast face detection architecture for auto-focus in smart-phones and digital cameras. <i>Science China Information Sciences</i> , 2016 , 59, 1	3.4	3
113	Dynamically reconfigurable architecture for symmetric ciphers. <i>Science China Information Sciences</i> , 2016 , 59, 1	3.4	5
112	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2015 , 23, 3085-3098	2.6	5
111	BriGuard: a lightweight indoor intrusion detection system based on infrared light spot displacement. <i>IET Science, Measurement and Technology</i> , 2015 , 9, 306-314	1.5	6

110	Efficient Fault-Tolerant Topology Reconfiguration Using a Maximum Flow Algorithm. <i>ACM Transactions on Reconfigurable Technology and Systems</i> , 2015 , 8, 1-24	2.7	5
109	Acceleration of control flows on reconfigurable architecture with a composite method 2015 ,		3
108	A 127 fps in full hd accelerator based on optimized AKAZE with efficiency and effectiveness for image feature extraction 2015 ,		7
107	Fast traffic sign recognition with a rotation invariant binary pattern based feature. <i>Sensors</i> , 2015 , 15, 2161-80	3.8	31
106	Configuration Approaches to Enhance Computing Efficiency of Coarse-Grained Reconfigurable Array. <i>Journal of Circuits, Systems and Computers</i> , 2015 , 24, 1550043	0.9	1
105	. <i>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</i> , 2015 , 34, 1264-1277	2.5	28
104	A Multi-modal 2D + 3D Face Recognition Method with a Novel Local Feature Descriptor 2015 ,		2
103	A Hybrid Reconfigurable Architecture and Design Methods Aiming at Control-Intensive Kernels. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2015 , 23, 1700-1709	2.6	5
102	A flexible and energy-efficient reconfigurable architecture for symmetric cipher processing 2015 ,		9
101	. <i>IEEE Transactions on Multimedia</i> , 2015 , 17, 1706-1720	6.6	27
100	Optimizing Spatial Mapping of Nested Loop for Coarse-Grained Reconfigurable Architectures. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2015 , 23, 2581-2594	2.6	8
99	Efficient memory partitioning for parallel data access in multidimensional arrays 2015 ,		19
98	A Stochastic Approach for the Analysis of Dynamic Fault Trees With Spare Gates Under Probabilistic Common Cause Failures. <i>IEEE Transactions on Reliability</i> , 2015 , 64, 878-892	4.6	25
97	. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2015 , 23, 1562-1566	2.6	17
96	Battery-Aware Loop Nests Mapping for CGRAs. <i>IEICE Transactions on Information and Systems</i> , 2015 , E98.D, 230-242	0.6	1
95	The Implementation of Texture-Based Video Up-Scaling on Coarse-Grained Reconfigurable Architecture. <i>IEICE Transactions on Information and Systems</i> , 2015 , E98.D, 276-287	0.6	1
94	Low-Power Loop Parallelization onto CGRA Utilizing Variable Dual VDD. <i>IEICE Transactions on Information and Systems</i> , 2015 , E98.D, 243-251	0.6	1
93	Mapping Multi-Level Loop Nests onto CGRAs Using Polyhedral Optimizations. <i>IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences</i> , 2015 , E98.A, 1419-1430	0.4	1

92	A 181 GOPS AKAZE Accelerator Employing Discrete-Time Cellular Neural Networks for Real-Time Feature Extraction. <i>Sensors</i> , 2015 , 15, 22509-29	3.8	2
91	A Novel 2D-to-3D Video Conversion Method Using Time-Coherent Depth Maps. <i>Sensors</i> , 2015 , 15, 15246-15264	3.8	6
90	High-Performance Motion Estimation for Image Sensors with Video Compression. <i>Sensors</i> , 2015 , 15, 20752-78	3.8	4
89	A novel approach using a minimum cost maximum flow algorithm for fault-tolerant topology reconfiguration in NoC architectures 2015 ,		5
88	Acceleration of nested conditionals on CGRAs via trigger scheme 2015 ,		4
87	A 83fps 1080P resolution 354 mW silicon implementation for computing the improved robust feature in affine space 2015 ,		1
86	. <i>IEEE Transactions on Multimedia</i> , 2015 , 17, 2354-2355	6.6	1
85	Neural approximating architecture targeting multiple application domains 2015 ,		4
84	A real-time time-consistent 2D-to-3D video conversion system using color histogram. <i>IEEE Transactions on Consumer Electronics</i> , 2015 , 61, 524-530	4.8	7
83	A Fast Integral Image Computing Hardware Architecture With High Power and Area Efficiency. <i>IEEE Transactions on Circuits and Systems II: Express Briefs</i> , 2015 , 62, 75-79	3.5	10
82	Reliability-aware mapping for various NoC topologies and routing algorithms under performance constraints. <i>Science China Information Sciences</i> , 2015 , 58, 1-14	3.4	3
81	A Flexible Energy- and Reliability-Aware Application Mapping for NoC-Based Reconfigurable Architectures. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2015 , 23, 2566-2580	2.6	14
80	2015 ,		2
79	RNA: A Reconfigurable Architecture for Hardware Neural Acceleration 2015 ,		2
78	2015 ,		2
77	Implementation of multi-standard video decoder on a heterogeneous coarse-grained reconfigurable processor. <i>Science China Information Sciences</i> , 2014 , 57, 1-14	3.4	
76	An uneven-dual-core processor based mobile platform for facilitating the collaboration among various embedded electronic devices. <i>IEEE Transactions on Consumer Electronics</i> , 2014 , 60, 137-145	4.8	
75	On-Chip Memory Hierarchy in One Coarse-Grained Reconfigurable Architecture to Compress Memory Space and to Reduce Reconfiguration Time and Data-Reference Time. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014 , 22, 983-994	2.6	17

74	Efficient and flexible memory architecture to alleviate data and context bandwidth bottlenecks of coarse-grained reconfigurable arrays. <i>Science China: Physics, Mechanics and Astronomy</i> , 2014 , 57, 2214-2227	3.6	2
73	An architecture of entropy decoder, inverse quantiser and predictor for multi-standard video decoding. <i>International Journal of Electronics</i> , 2014 , 101, 877-893	1.2	
72	SimRPU: A Simulation Environment for Reconfigurable Architecture Exploration. <i>IEEE Transactions on Very Large Scale Integration (VLSI) Systems</i> , 2014 , 22, 2635-2648	2.6	17
71	. <i>IEEE Transactions on Reliability</i> , 2014 , 63, 480-494	4.6	21
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1 A VLSI architecture of spatial combinative lifting algorithm based 2-D DWT/IDWT

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