Leibo Liu

List of Publications by Citations

253 papers	2,193 citations	22 h-index	37 g-index
340 ext. papers	3,095 ext. citations	2.8 avg, IF	5.37 L-index

#	Paper	IF	Citations
253	FP-BNN: Binarized neural network on FPGA. *Neurocomputing*, **2018**, 275, 1072-1086	5.4	138
252	Deep Convolutional Neural Network Architecture With Reconfigurable Computation Patterns. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2220-2233	2.6	132
251	A Review, Classification, and Comparative Evaluation of Approximate Arithmetic Circuits. *ACM Journal on Emerging Technologies in Computing Systems*, **2017**, 13, 1-34	1.7	104
250	A High Energy Efficient Reconfigurable Hybrid Neural Network Processor for Deep Learning Applications. *IEEE Journal of Solid-State Circuits*, **2018**, 53, 968-982	5.5	101
249	Analog circuit optimization system based on hybrid evolutionary algorithms. *The Integration VLSI Journal*, **2009**, 42, 137-148	1.4	84
248	A Crop Monitoring System Based on Wireless Sensor Network. *Procedia Environmental Sciences*, **2011**, 11, 558-565		64
247	Approximate Arithmetic Circuits: A Survey, Characterization, and Recent Applications. *Proceedings of the IEEE*, **2020**, 108, 2108-2135	14.3	39
246	A 1.06-to-5.09 TOPS/W reconfigurable hybrid-neural-network processor for deep learning applications **2017**,		37
245	An Implementation of Fast-Locking and Wide-Range 11-bit Reversible SAR DLL. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2010**, 57, 421-425	3.5	36
244	Polyhedral model based mapping optimization of loop nests for CGRAs **2013**,		35
243	A Survey of Coarse-Grained Reconfigurable Architecture and Design. *ACM Computing Surveys*, **2020**, 52, 1-39	13.4	34
242	An Energy-Efficient Reconfigurable Processor for Binary-and Ternary-Weight Neural Networks With Flexible Data Bit Width. *IEEE Journal of Solid-State Circuits*, **2019**, 54, 1120-1136	5.5	32
241	Fast traffic sign recognition with a rotation invariant binary pattern based feature. *Sensors*, **2015**, 15, 2161-80	3.8	31
240	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2015**, 34, 1264-1277	2.5	28
239	. *IEEE Transactions on Multimedia*, **2015**, 17, 1706-1720	6.6	27
238	RANA: Towards Efficient Neural Acceleration with Refresh-Optimized Embedded DRAM **2018**,		27
237	A Stochastic Approach for the Analysis of Dynamic Fault Trees With Spare Gates Under Probabilistic Common Cause Failures. *IEEE Transactions on Reliability*, **2015**, 64, 878-892	4.6	25

236	. *IEEE Journal of Solid-State Circuits*, **2004**, 39, 2032-2040	5.5	25
235	A 141 UW, 2.46 PJ/Neuron Binarized Convolutional Neural Network Based Self-Learning Speech Recognition Processor in 28NM CMOS **2018**,		24
234	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 1717-1730	3.9	23
233	A High-Performance and Energy-Efficient FIR Adaptive Filter Using Approximate Distributed Arithmetic Circuits. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 313-326	3.9	23
232	A High Throughput Acceleration for Hybrid Neural Networks With Efficient Resource Management on FPGA. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 678-691	2.5	23
231	Memory-Aware Loop Mapping on Coarse-Grained Reconfigurable Architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1895-1908	2.6	22
230	Algorithm and Architecture of a Low-Complexity and High-Parallelism Preprocessing-Based K -Best Detector for Large-Scale MIMO Systems. *IEEE Transactions on Signal Processing*, **2018**, 66, 1860-1875	4.8	21
229	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2519-2529	2.5	21
228	. *IEEE Transactions on Reliability*, **2014**, 63, 480-494	4.6	21
227	An Ultra-Low Power Binarized Convolutional Neural Network-Based Speech Recognition Processor With On-Chip Self-Learning. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 4648-4661	3.9	20
226	**2019**,		20
225	Efficient memory partitioning for parallel data access in multidimensional arrays **2015**,		19
224	Low-Computing-Load, High-Parallelism Detection Method Based on Chebyshev Iteration for Massive MIMO Systems With VLSI Architecture. *IEEE Transactions on Signal Processing*, **2017**, 65, 3775-3788	4.8	18
223	. *IEEE Transactions on Signal Processing*, **2020**, 68, 573-588	4.8	18
222	An Energy-Efficient and Noise-Tolerant Recurrent Neural Network Using Stochastic Computing. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2213-2221	2.6	18
221	Stochastic Analysis of Multiplex Boolean Networks for Understanding Epidemic Propagation. *IEEE Access*, **2018**, 6, 35292-35304	3.5	18
220	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1562-1566	2.6	17
219	On-Chip Memory Hierarchy in One Coarse-Grained Reconfigurable Architecture to Compress Memory Space and to Reduce Reconfiguration Time and Data-Reference Time. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 983-994	2.6	17

218	SimRPU: A Simulation Environment for Reconfigurable Architecture Exploration. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2635-2648	2.6	17
217	A Multi-Objective Model Oriented Mapping Approach for NoC-based Computing Systems. *IEEE Transactions on Parallel and Distributed Systems*, **2017**, 28, 662-676	3.7	17
216	Evolver: A Deep Learning Processor With On-Device Quantization Voltage Frequency Tuning. *IEEE Journal of Solid-State Circuits*, **2021**, 56, 658-673	5.5	17
215	Reliability Evaluation of Phased-Mission Systems Using Stochastic Computation. *IEEE Transactions on Reliability*, **2016**, 65, 1612-1623	4.6	16
214	Large-scale MIMO detection design and FPGA implementations using SOR method **2016**,		16
213	Exploration of Benes Network in Cryptographic Processors: A Random Infection Countermeasure for Block Ciphers Against Fault Attacks. *IEEE Transactions on Information Forensics and Security*, **2017**, 12, 309-322	8	16
212	Design of wireless multi-media sensor network for precision agriculture. *China Communications*, **2013**, 10, 71-88	3	15
211	HReA: An Energy-Efficient Embedded Dynamically Reconfigurable Fabric for 13-Dwarfs Processing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 381-385	3.5	14
210	Against Double Fault Attacks: Injection Effort Model, Space and Time Randomization Based Countermeasures for Reconfigurable Array Architecture. *IEEE Transactions on Information Forensics and Security*, **2016**, 11, 1151-1164	8	14
209	. *IEEE Transactions on Computers*, **2019**, 68, 1635-1646	2.5	14
208	A fault tolerant NoC architecture using quad-spare mesh topology and dynamic reconfiguration. *Journal of Systems Architecture*, **2013**, 59, 482-491	5.5	14
207	A Flexible Energy- and Reliability-Aware Application Mapping for NoC-Based Reconfigurable Architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2566-2580	2.6	14
206	An energy-efficient coarse-grained dynamically reconfigurable fabric for multiple-standard video decoding applications **2013**,		13
205	. *IEEE Transactions on Wireless Communications*, **2020**, 19, 1025-1037	9.6	13
204	Gradient Descent Using Stochastic Circuits for Efficient Training of Learning Machines. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 2530-2541	2.5	13
203	. *IEEE Transactions on Multimedia*, **2019**, 21, 943-956	6.6	12
202	An AdaBoost-Based Face Detection System Using Parallel Configurable Architecture With Optimized Computation. *IEEE Systems Journal*, **2017**, 11, 260-271	4.3	11
201	**2018**,		11

200	Bit-Width Based Resource Partitioning for CNN Acceleration on FPGA **2017**,		11
199	Compiler Framework for Reconfigurable Computing Architecture. *IEICE Transactions on Electronics*, **2009**, E92-C, 1284-1290	0.4	11
198	Characterizing Approximate Adders and Multipliers Optimized under Different Design Constraints **2019**,		10
197	Multibank memory optimization for parallel data access in multiple data arrays **2016**,		10
196	A Fast Integral Image Computing Hardware Architecture With High Power and Area Efficiency. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2015**, 62, 75-79	3.5	10
195	CIACP: A Correlation- and Iteration- Aware Cache Partitioning Mechanism to Improve Performance of Multiple Coarse-Grained Reconfigurable Arrays. *IEEE Transactions on Parallel and Distributed Systems*, **2017**, 28, 29-43	3.7	9
194	A flexible and energy-efficient reconfigurable architecture for symmetric cipher processing **2015**,		9
193	Low-Power Reconfigurable Processor Utilizing Variable Dual $V_{rm DD}$. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2013**, 60, 217-221	3.5	9
192	Aggressive Pipelining of Irregular Applications on Reconfigurable Hardware **2017**,		9
191	AEPE: An area and power efficient RRAM crossbar-based accelerator for deep CNNs **2017**,		9
190	A multi-modal face recognition method using complete local derivative patterns and depth maps. *Sensors*, **2014**, 14, 19561-81	3.8	9
189	Conflict-Free Loop Mapping for Coarse-Grained Reconfigurable Architecture with Multi-Bank Memory. *IEEE Transactions on Parallel and Distributed Systems*, **2017**, 28, 2471-2485	3.7	8
188	A General Pattern-Based Dynamic Compilation Framework for Coarse-Grained Reconfigurable Architectures **2019**,		8
187	Optimizing Spatial Mapping of Nested Loop for Coarse-Grained Reconfigurable Architectures. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2581-2594	2.6	8
186	. *IEEE Transactions on Parallel and Distributed Systems*, **2016**, 27, 3199-3213	3.7	8
185	A Multi-Task Hardwired Accelerator for Face Detection and Alignment. *IEEE Transactions on Circuits and Systems for Video Technology*, **2020**, 30, 4284-4298	6.4	8
184	Data-Flow Graph Mapping Optimization for CGRA With Deep Reinforcement Learning. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 2271-2283	2.5	8
183	A 135-frames/s 1080p 87.5-mW Binary-Descriptor-Based Image Feature Extraction Accelerator. *IEEE Transactions on Circuits and Systems for Video Technology*, **2016**, 26, 1532-1543	6.4	7

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181	LCP **2018**,		7
180	A real-time time-consistent 2D-to-3D video conversion system using color histogram. *IEEE Transactions on Consumer Electronics*, **2015**, 61, 524-530	4.8	7
179	Complex division and square-root using CORDIC **2012**,		7
178	Parallelization of Computing-Intensive Tasks of the H.264 High Profile Decoding Algorithm on a Reconfigurable Multimedia System. *IEICE Transactions on Information and Systems*, **2010**, E93-D, 3223-3231	0.6	7
177	LWRpro: An Energy-Efficient Configurable Crypto-Processor for Module-LWR. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 1146-1159	3.9	7
176	. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 1217-1230	3.9	7
175	An Ultra-High Energy-Efficient Reconfigurable Processor for Deep Neural Networks with Binary/Ternary Weights in 28NM CMOS **2018**,		7
174	TLIA: Efficient Reconfigurable Architecture for Control-Intensive Kernels with Triggered-Long-Instructions. *IEEE Transactions on Parallel and Distributed Systems*, **2016**, 27, 2143-2154	3.7	6
173	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 507-520	2.6	6
172	BriGuard: a lightweight indoor intrusion detection system based on infrared light spot displacement. *IET Science, Measurement and Technology*, **2015**, 9, 306-314	1.5	6
171	DFGNet: Mapping dataflow graph onto CGRA by a deep learning approach **2017**,		6
170	Data cache prefetching via context directed pattern matching for coarse-grained reconfigurable arrays **2016**,		6
169	Joint Modulo Scheduling and $V_{mathrm{ dd}}$ Assignment for Loop Mapping on Dual-$V_{mathrm{ dd}}$ CGRAs. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2016**, 35, 1475-1488	2.5	6
168	A Novel 2D-to-3D Video Conversion Method Using Time-Coherent Depth Maps. *Sensors*, **2015**, 15, 15246-15264	3.4	6
167	A VLSI design of sensor node for wireless image sensor network **2010**,		6
166	A Fast and Power-Efficient Hardware Architecture for Non-Maximum Suppression. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 1870-1874	3.5	5
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164	Efficient Fault-Tolerant Topology Reconfiguration Using a Maximum Flow Algorithm. *ACM Transactions on Reconfigurable Technology and Systems*, **2015**, 8, 1-24	2.7	5
163	A Hybrid Reconfigurable Architecture and Design Methods Aiming at Control-Intensive Kernels. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 1700-1709	2.6	5
162	A Coarse-Grained Reconfigurable Architecture for Compute-Intensive MapReduce Acceleration. *IEEE Computer Architecture Letters*, **2016**, 15, 69-72	1.8	5
161	Trigger-Centric Loop Mapping on CGRAs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 1998-2002	2.6	5
160	A novel approach using a minimum cost maximum flow algorithm for fault-tolerant topology reconfiguration in NoC architectures **2015**,		5
159	Configuration Context Reduction for Coarse-Grained Reconfigurable Architecture. *IEICE Transactions on Information and Systems*, **2012**, E95-D, 335-344	0.6	5
158	Reconfiguration Process Optimization of Dynamically Coarse Grain Reconfigurable Architecture for Multimedia Applications. *IEICE Transactions on Information and Systems*, **2012**, E95.D, 1858-1871	0.6	5
157	A Cycle-Accurate Simulator for a Reconfigurable Multi-Media System. *IEICE Transactions on Information and Systems*, **2010**, E93-D, 3202-3210	0.6	5
156	Aggressive Pipelining of Irregular Applications on Reconfigurable Hardware. *Computer Architecture News*, **2017**, 45, 575-586		5
155	. *IEEE Journal of Solid-State Circuits*, **2020**, 55, 505-519	5.5	5
154	Dynamically reconfigurable architecture for symmetric ciphers. *Science China Information Sciences*, **2016**, 59, 1	3.4	5
153	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 208-219	2.5	5
152	. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 782-795	2.5	5
151	Energy-aware loops mapping on multi-vdd CGRAs without performance degradation **2017**,		4
150	A 1.17 TOPS/W, 150fps Accelerator for Multi-Face Detection and Alignment **2019**,		4
149	High-Performance Motion Estimation for Image Sensors with Video Compression. *Sensors*, **2015**, 15, 20752-78	3.2	4
148	Acceleration of nested conditionals on CGRAs via trigger scheme **2015**,		4
147	Neural approximating architecture targeting multiple application domains **2015**,		4

146	Motion-sensor fusion-based gesture recognition and its VLSI architecture design for mobile devices. *International Journal of Electronics*, **2014**, 101, 621-635	1.2	4
145	Optimization of speeded-up robust feature algorithm for hardware implementation. *Science China Information Sciences*, **2014**, 57, 1-15	3.4	4
144	Hybrid Wired/Wireless On-Chip Network Design for Application-Specific SoC. *IEICE Transactions on Electronics*, **2012**, E95.C, 495-505	0.4	4
143	**2013**,		4
142	A high-throughput fixed-point complex divider for FPGAs. *IEICE Electronics Express*, **2013**, 10, 20120879-20120879	0.5	4
141	A reconfigurable multi-processor SoC for media applications **2010**,		4
140	Multi-CNN and decision tree based driving behavior evaluation **2017**,		4
139	User Behavior Pattern Analysis and Prediction Based on Mobile Phone Sensors. *Lecture Notes in Computer Science*, **2010**, 177-189	0.9	4
138	Joint loop mapping and data placement for coarse-grained reconfigurable architecture with multi-bank memory **2016**,		4
137	Acceleration of control flows on reconfigurable architecture with a composite method **2015**,		3
136	Stress-Aware Loops Mapping on CGRAs with Dynamic Multi-Map Reconfiguration. *IEEE Transactions on Parallel and Distributed Systems*, **2018**, 29, 2105-2120	3.7	3
135	Anole: A Highly Efficient Dynamically Reconfigurable Crypto-Processor for Symmetric-Key Algorithms. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 3081-3094	2.5	3
134	**2016**,		3
133	Bit-width Adaptive Accelerator Design for Convolution Neural Network **2018**,		3
132	A Face Alignment Accelerator Based on Optimized Coarse-to-Fine Shape Searching. *IEEE Transactions on Circuits and Systems for Video Technology*, **2019**, 29, 2467-2481	6.4	3
131	Parana: A Parallel Neural Architecture Considering Thermal Problem of 3D Stacked Memory. *IEEE Transactions on Parallel and Distributed Systems*, **2019**, 30, 146-160	3.7	3
130	A Lifetime Reliability-Constrained Runtime Mapping for Throughput Optimization in Many-Core Systems. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2019**, 38, 1771-1784	2.5	3
129	Reliability-aware mapping for various NoC topologies and routing algorithms under performance constraints. *Science China Information Sciences*, **2015**, 58, 1-14	3.4	3

128	Map-reduce inspired loop parallelization on CGRA **2014**,		3
127	**2014**,		3
126	A parallel hardware architecture for fast integral image computing **2014**,		3
125	Battery-Aware MAC Analytical Modeling for Extending Lifetime of Low Duty-Cycled Wireless Sensor Network **2013**,		3
124	Mapping Optimization of Affine Loop Nests for Reconfigurable Computing Architecture. *IEICE Transactions on Information and Systems*, **2012**, E95.D, 2898-2907	0.6	3
123	A VLSI architecture of spatial combinative lifting algorithm based 2-D DWT/IDWT		3
122	Learning Convolutional Neural Networks for Data-Flow Graph Mapping on Spatial Programmable Architectures (Abstract Only) **2017**,		3
121	Dynamic Frequency Scaling Aware Opportunistic Through-Silicon-Via Inductor Utilization in Resonant Clocking. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 281-293	2.5	3
120	NTTU: An Area-Efficient Low-Power NTT-Uncoupled Architecture for NTT-Based Multiplication. *IEEE Transactions on Computers*, **2020**, 69, 520-533	2.5	3
119	TFE: Energy-efficient Transferred Filter-based Engine to Compress and Accelerate Convolutional Neural Networks **2020**,		3
118	An Implementation of Multiple-Standard Video Decoder on a Mixed-Grained Reconfigurable Computing Platform. *IEICE Transactions on Information and Systems*, **2016**, E99.D, 1285-1295	0.6	3
117	A fast face detection architecture for auto-focus in smart-phones and digital cameras. *Science China Information Sciences*, **2016**, 59, 1	3.4	3
116	**2019**,		3
115	Reconfigurable Architecture for Neural Approximation in Multimedia Computing. *IEEE Transactions on Circuits and Systems for Video Technology*, **2019**, 29, 892-906	6.4	3
114	A 60 Gb/s-Level Coarse-Grained Reconfigurable Cryptographic Processor With Less Than 1-W Power. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 375-379	3.5	3
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112	On-Chip Trust Evaluation Utilizing TDC-Based Parameter-Adjustable Security Primitive. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2021**, 40, 1985-1994	2.5	3
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109	Linear Massive MIMO Detection Algorithm **2019**, 71-123		2
108	A Multi-modal 2D + 3D Face Recognition Method with a Novel Local Feature Descriptor **2015**,		2
107	Hardware efficient signal detector based on lanczos method for massive MIMO systems **2017**,		2
106	A Fast and Power-Efficient Hardware Architecture for Visual Feature Detection in Affine-SIFT. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 3362-3375	3.9	2
105	Memory Partitioning for Parallel Multipattern Data Access in Multiple Data Arrays. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 431-444	2.5	2
104	CDPM: Context-Directed Pattern Matching Prefetching to Improve Coarse-Grained Reconfigurable Array Performance. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2018**, 37, 1171-1184	2.5	2
103	MSAM: A Multi-Layer Bi-LSTM Based Speech to Vector Model with Residual Attention Mechanism **2019**,		2
102	Addition Circuit optimization Using Carry-Lookahead and SIMD for Homomorphic Encryption **2019**,		2
101	Efficient and flexible memory architecture to alleviate data and context bandwidth bottlenecks of coarse-grained reconfigurable arrays. *Science China: Physics, Mechanics and Astronomy*, **2014**, 57, 2214-2227	3.6	2
100	A 700fps Optimized Coarse-to-Fine Shape Searching Based Hardware Accelerator for Face Alignment **2017**,		2
99	Implementation of in-loop filter for HEVC decoder on reconfigurable processor. *IET Image Processing*, **2017**, 11, 685-692	1.7	2
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96	A VLSI architecture for enhancing the fault tolerance of NoC using quad-spare mesh topology and dynamic reconfiguration **2013**,		2
95	Battery-Aware Task Mapping for Coarse-Grained Reconfigurable Architecture. *IEICE Transactions on Information and Systems*, **2013**, E96.D, 2524-2535	0.6	2
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93	A fast complete deblocking filter on a coarse-grained reconfigurable processor supporting H.264 high profile decoding **2010**,		2

92	Mixed-level modeling for network on chip infrastructure in SoC design **2010**,		2
91	Compiler framework for reconfigurable computing system **2009**,		2
90	Reducing configuration contexts for coarse-grained reconfigurable architecture **2012**,		2
89	Energy-aware task partitioning and scheduling algorithm for reconfigurable processor **2012**,		2
88	Multi-Battery Scheduling for Battery-Powered DVS Systems. *IEICE Transactions on Communications*, **2012**, E95.B, 2278-2285	0.5	2
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85	RNA: A Reconfigurable Architecture for Hardware Neural Acceleration **2015**,		2
84	**2015**,		2
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82	Achieving Flexible Global Reconfiguration in NoCs Using Reconfigurable Rings. *IEEE Transactions on Parallel and Distributed Systems*, **2020**, 31, 611-622	3.7	2
81	Pattern-Based Dynamic Compilation System for CGRAs With Online Configuration Transformation. *IEEE Transactions on Parallel and Distributed Systems*, **2020**, 31, 2981-2994	3.7	2
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78	Optimal design of a low-power, phase-switching modulator for implantable medical applications. *The Integration VLSI Journal*, **2019**, 69, 289-300	1.4	1
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76	Architecture, challenges and applications of dynamic reconfigurable computing. *Journal of Semiconductors*, **2020**, 41, 021401	2.3	1
75	Multi-Bank Memory Aware Force Directed Scheduling for High-Level Synthesis. *IEEE Access*, **2018**, 6, 7526-7540	3.5	1

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71	Row-based configuration mechanism for a 2-D processing element array in coarse-grained reconfigurable architecture. *Science China Information Sciences*, **2014**, 57, 1-18	3.4	1
70	A WiSN node SoC with real-time image compressor and IEEE 802.15.4 MAC accelerator. *International Journal of Electronics*, **2014**, 101, 1580-1594	1.2	1
69	A high performance parallel computing architecture for robust image features. *International Journal of Electronics*, **2014**, 101, 391-404	1.2	1
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67	PMCC: Fast and Accurate System-Level Power Modeling for Processors on Heterogeneous SoC. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2017**, 64, 540-544	3.5	1
66	Reconfigurable VLSI Architecture for Real-Time 2D-to-3D Conversion. *IEEE Access*, **2017**, 5, 26604-26613	3.5	1
65	Memory fartitioning-based modulo scheduling for high-level synthesis **2017**,		1
64	An efficient hardware design for cerebellar models using approximate circuits **2017**,		1
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60	Mapping Multi-Level Loop Nests onto CGRAs Using Polyhedral Optimizations. *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, **2015**, E98.A, 1419-1430	0.4	1
59	A 83fps 1080P resolution 354 mW silicon implementation for computing the improved robust feature in affine space **2015**,		1
58	. *IEEE Transactions on Multimedia*, **2015**, 17, 2354-2355	6.6	1
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56	Hierarchical Pipeline Optimization of Coarse Grained Reconfigurable Processor for Multimedia Applications **2014**,		1
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