

# Cong Xu

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/12156810/publications.pdf>

Version: 2024-02-01

16  
papers

2,490  
citations

2682572

2  
h-index

2917675

2  
g-index

16  
all docs

16  
docs citations

16  
times ranked

1715  
citing authors

#	ARTICLE	IF	CITATIONS
1	PRIME. Computer Architecture News, 2016, 44, 27-39.	2.5	823
2	NVSim: A Circuit-Level Performance, Energy, and Area Model for Emerging Nonvolatile Memory. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 994-1007.	2.7	778
3	Pinatubo. , 2016, , .		314
4	Overcoming the challenges of crossbar resistive memory architectures. , 2015, , .		233
5	Understanding the trade-offs in multi-level cell ReRAM memory design. , 2013, , .		100
6	Design trade-offs for high density cross-point resistive memory. , 2012, , .		70
7	Design implications of memristor-based RRAM cross-point structures. , 2011, , .		56
8	Design of cross-point metal-oxide ReRAM emphasizing reliability and cost. , 2013, , .		35
9	Device-architecture co-optimization of STT-RAM based memory for low power embedded systems. , 2011, , .		20
10	Building energy-efficient multi-level cell STT-MRAM based cache through dynamic data-resistance encoding. , 2014, , .		20
11	Using multi-level cell STT-RAM for fast and energy-efficient local checkpointing. , 2014, , .		16
12	Bandwidth-aware reconfigurable cache design with hybrid memory technologies. , 2011, , .		9
13	When to forget: A system-level perspective on STT-RAMs. , 2012, , .		9
14	Modeling framework for cross-point resistive memory design emphasizing reliability and variability issues. , 2015, , .		5
15	Lazy Precharge: An overhead-free method to reduce precharge overhead for memory parallelism improvement of DRAM system. , 2013, , .		2
16	Modeling and design exploration of FBDRAM as on-chip memory. , 2012, , .		0