Nacho Navarro

List of Publications by Year
in descending order

20 papers	**489** citations

1163117

8 h-index	

1281871

11 g-index	

21 all docs	**21** docs citations
21 times ranked	**403** citing authors

#	Article	IF	Citations
1	Decomposable and responsive power models for multicore processors using performance counters. , 2010, , .		107
2	DiDi: Mitigating the Performance Impact of TLB Shootdowns Using a Shared TLB Directory. , 2011, , .		64
3	TERAFLUX: Harnessing dataflow in next generation teradevices. Microprocessors and Microsystems, 2014, 38, 976-990.	2.8	56
4	Assessing Accelerator-Based HPC Reverse Time Migration. IEEE Transactions on Parallel and Distributed Systems, 2011, 22, 147-162.	5.6	49
5	Energy accounting for shared virtualized environments under DVFS using PMC-based power models. Future Generation Computer Systems, 2012, 28, 457-468.	7.5	35
6	NanosCompiler: supporting flexible multilevel parallelism exploitation in OpenMP. Concurrency and Computation: Practice and Experience, 2000, 12, 1205-1218.	0.5	27
7	CODOMs. Computer Architecture News, 2014, 42, 469-480.	2.5	22
8	Counter-Based Power Modeling Methods: Top-Down vs. Bottom-Up. Computer Journal, 2013, 56, 198-213.	2.4	21
9	Exploiting memory customization in FPGA for 3D stencil computations. , 2009, , .		16
10	The AXIOM software layers. Microprocessors and Microsystems, 2016, 47, 262-277.	2.8	12
11	The AXIOM Software Layers. , 2015, , .		11
12	The AXIOM project (Agile, eXtensible, fast I/O Module). , 2015, , .		11
13	Direct Inter-Process Communication (dIPC). , 2017, , .		11
14	High-Performance Reverse Time Migration on GPU. , 2009, , .		10
15	Hardwareâ€"Software Coherence Protocol for the Coexistence of Caches and Local Memories. IEEE Transactions on Computers, 2015, 64, 152-165.	3.4	5
16	TARCAD: A template architecture for reconfigurable accelerator designs. , 2011, , .		2
17	POTRA. , 2012, , .		2
18	A template system for the efficient compilation of domain abstractions onto reconfigurable computers. Journal of Systems Architecture, 2013, 59, 91-102.	4.3	1

#	Article	IF	Citations
19	Adaptive Runtime-Assisted Block Prefetching on Chip-Multiprocessors. International Journal of Parallel Programming, 2017, 45, 530-550.	1.5	1
20	POTRA. Performance Evaluation Review, 2012, 40, 427-428.	0.6	0