

Chunsheng Jiang

List of Publications by Year in descending order

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1417
citing authors

#	ARTICLE	IF	CITATIONS
1	Atomic threshold-switching enabled MoS ₂ transistors towards ultralow-power electronics. Nature Communications, 2020, 11, 6207.	12.8	52
2	Logic “AND” and “OR” realized in a single intelligent three dimension transistor. Applied Physics Express, 2019, 12, 104004.	2.4	1
3	Negative Capacitance Oxide Thin-Film Transistor With Sub-60 mV/Decade Subthreshold Swing. IEEE Electron Device Letters, 2019, 40, 826-829.	3.9	26
4	Proton Conductor Gated Synaptic Transistor Based on Transparent IGZO for Realizing Electrical and UV Light Stimulus. IEEE Journal of the Electron Devices Society, 2019, 7, 38-45.	2.1	24
5	A Closed Form Analytical Model of Back-Gated 2-D Semiconductor Negative Capacitance Field Effect Transistors. IEEE Journal of the Electron Devices Society, 2018, 6, 189-194.	2.1	35
6	Steep-slope hysteresis-free negative capacitance MoS ₂ transistors. Nature Nanotechnology, 2018, 13, 24-28.	31.5	422
7	Effects of parasitic capacitance on both static and dynamic electrical characteristics of back-gated two-dimensional semiconductor negative-capacitance field-effect transistors. Applied Physics Express, 2018, 11, 124101.	2.4	4
8	Subthreshold Behaviors of Nanoscale Silicon and Germanium Junctionless Cylindrical Surrounding-Gate MOSFETs. ChemistrySelect, 2018, 3, .	1.5	1
9	MoS ₂ Negative Capacitance Field Effect Transistors with Subthreshold Swing below the Physics Limit. Advanced Materials, 2018, 30, e1800932.	21.0	87
10	Steep-Slope WSe ₂ Negative Capacitance Field-Effect Transistor. Nano Letters, 2018, 18, 3682-3687.	9.1	97
11	An analytical charge-sheet drain current model for monolayer transition metal dichalcogenide negative capacitance field-effect transistors. , 2017, , .		1
12	Thin, Transferred Layers of Silicon Dioxide and Silicon Nitride as Water and Ion Barriers for Implantable Flexible Electronic Systems. Advanced Electronic Materials, 2017, 3, 1700077.	5.1	61
13	Analytical drain current model for long-channel double-gate negative capacitance junctionless transistors using Landau theory. , 2016, , .		0
14	Simulation-based study of negative capacitance double-gate junctionless transistors with ferroelectric gate dielectric. Solid-State Electronics, 2016, 126, 130-135.	1.4	25
15	Investigation of Negative Capacitance Gate-all-around Tunnel FETs Combining Numerical Simulation and Analytical Modeling. IEEE Nanotechnology Magazine, 2016, , 1-1.	2.0	28
16	Analytical drain current model for long-channel gate-all-around negative capacitance transistors with a metal “ferroelectric” insulator “semiconductor” structure. Japanese Journal of Applied Physics, 2016, 55, 024201.	1.5	27
17	A carrier-based analytic theory for electrical simulation of negative capacitance surrounding gate ferroelectric capacitor. , 2015, , .		1
18	A carrier-based analytical theory for negative capacitance symmetric double-gate field effect transistors and its simulation verification. Journal Physics D: Applied Physics, 2015, 48, 365103.	2.8	22

#	ARTICLE	IF	CITATIONS
19	A rigorous analytical model for short-channel junctionless double-gate MOSFETs. , 2014, , .		0
20	Investigation of the junctionless line tunnel field-effect transistor. , 2014, , .		2