

Michael Graef

List of Publications by Year in descending order

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16
papers

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1937685

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docs citations

16
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164
citing authors

#	ARTICLE	IF	CITATIONS
1	Compact Model for Short-Channel Junctionless Accumulation Mode Double Gate MOSFETs. IEEE Transactions on Electron Devices, 2014, 61, 288-299.	3.0	95
2	A 2D closed form model for the electrostatics in hetero-junction double-gate tunnel-FETs for calculation of band-to-band tunneling current. Microelectronics Journal, 2014, 45, 1144-1153.	2.0	26
3	Modeling and performance study of nanoscale double gate junctionless and inversion mode MOSFETs including carrier quantization effects. Microelectronics Journal, 2014, 45, 1220-1225.	2.0	9
4	Advanced analytical modeling of double-gate Tunnel-FETs – A performance evaluation. Solid-State Electronics, 2018, 141, 31-39.	1.4	9
5	Improved analytical potential modeling in double-gate tunnel-FETs. , 2014, , .		8
6	Implementation of a DC compact model for double-gate Tunnel-FET based on 2D calculations and application in circuit simulation. , 2016, , .		8
7	Two-dimensional modeling of an ultra-thin body single-gate Si Tunnel-FET. , 2014, , .		6
8	Model for investigation of I_{on}/I_{off} ratios in short-channel junctionless double gate MOSFETs. , 2013, , .		4
9	Numerical analysis and analytical modeling of RDF in DG Tunnel-FETs. , 2016, , .		4
10	Analytical approach to consider Gaussian junction profiles in compact models of tunnel-FETs. , 2015, , .		3
11	Wavelet-based calculation of the transmission coefficient for tunneling events in Tunnel-FETs. , 2015, , .		3
12	Comparative numerical analysis and analytical RDF-modeling of MOSFETs and DG Tunnel-FETs. , 2016, , .		3
13	Two-dimensional bias dependent model for the screening length in double-gate Tunnel-FETs. , 2013, , .		2
14	Modeling approach for rapid NEGF-based simulation of ballistic current in ultra-short DG MOSFETs. , 2016, , .		2
15	Static noise margin analysis of 8T TFET SRAM cells using a 2D compact model adapted to measurement data of fabricated TFET devices. , 2017, , .		2
16	DC/AC Compact Modeling of TFETs for Circuit Simulation of Logic Cells Based on an Analytical Physics-Based Framework. , 2017, , .		0