Kazuaki Murakami

List of Publications by Year
in descending order

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22 papers	104 citations	1478505 6 h-index	1474206 9 g-index
22 all docs	22 docs citations	22 times ranked	68 citing authors

#	Article	IF	Citations
1	A Reconfigurable Data-Path Accelerator Based on Single Flux Quantum Circuits. IEICE Transactions on Electronics, 2014, E97.C, 141-148.	0.6	2
2	Performance evaluation of 3D stacked multi-core processors with temperature consideration. , 2012, , .		2
3	Improving performance and energy efficiency ofÂembedded processors via post-fabrication instruction set customization. Journal of Supercomputing, 2012, 60, 196-222.	3.6	7
4	Hardware and software requirements for implementing a high-performance superconductivity circuits-based accelerator. , 2011, , .		1
5	A design scheme for a reconfigurable accelerator implemented by single-flux quantum circuits. Journal of Systems Architecture, 2011, 57, 169-179.	4.3	6
6	Routing architecture and algorithms for a superconductivity circuits-based computing hardware. , 2011, , .		0
7	3D implemented SRAM/DRAM hybrid cache architecture for high-performance and low power consumption. , 2011, , .		3
8	Mapping scientific applications on a large-scale data-path accelerator implemented by single-flux quantum (SFQ) circuits. , 2010, , .		2
9	A Dynamic Solution for Efficient MPI Collective Communications. , 2009, , .		1
10	A robust dynamic optimization for MPI Alltoall operation. , 2009, , .		1
11	An Operand Routing Network for an SFQ Reconfigurable Data-Paths Processor. IEEE Transactions on Applied Superconductivity, 2009, 19, 665-669.	1.7	18
12	An architecture framework for an adaptive extensible processor. Journal of Supercomputing, 2008, 45, 313-340.	3.6	18
13	An Integrated Temporal Partitioning and Mapping Framework for Handling Custom Instructions on a Reconfigurable Functional Unit. Lecture Notes in Computer Science, 2006, , 219-230.	1.3	5
14	A Reconfigurable Functional Unit for an Adaptive Dynamic Extensible Processor. , 2006, , .		8
15	Custom Instruction Generation Using Temporal Partitioning Techniques for a Reconfigurable Functional Unit. Lecture Notes in Computer Science, 2006, , 722-731.	1.3	8
16	Development of Special Purpose Computers for Various Kinds of Chemical Simulations. Journal of Computer Chemistry Japan, 2006, 5, 131-138.	0.1	0
17	The optimum pipeline depth of a microprocessor for low energy consumption. Electronics and Communications in Japan, 2005, 88, 1-11.	0.2	0
18	An analysis about increasable latch overhead time for processor pipeline depth increase. Electronics and Communications in Japan, Part III: Fundamental Electronic Science (English Translation of Denshi) Tj ETQq0 0 0 rgBT /Overlock 10 Tf		2

#	Article	IF	Citations
19	Development of a Special-Purpose Processor for Molecular Orbital Calculations. Journal of Computer Chemistry Japan, 2005, 4, 155-164.	0.1	4
20	Development of Special Purpose Computers for Various Kinds of Chemical Simulations. Journal of Computer Chemistry Japan, 2005, 4, 131-138.	0.1	2
21	Synthesis of an Affinity Adsorbent for Sialidase. Journal of Carbohydrate Chemistry, 1993, 12, 201-208.	1.1	8
22	DSNS (dynamically-hazard-resolved statically-code-scheduled, nonuniform superscalar). Computer Architecture News, 1991, 19, 14-29.	2.5	6