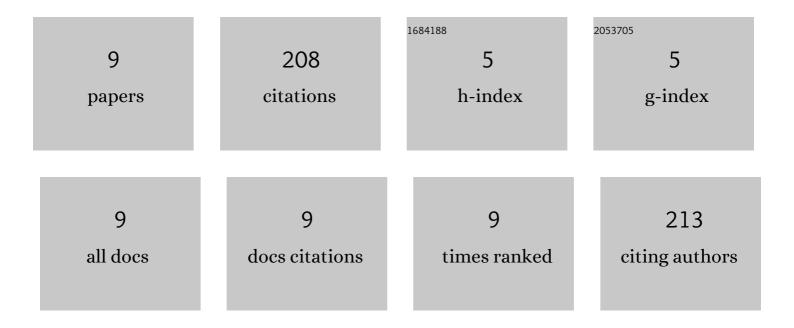
Ahmet Ceyhan

List of Publications by Year in descending order

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Δημετ Γεγηνη

#	Article	IF	CITATIONS
1	Adapting Interconnect Technology to Multigate Transistors for Optimum Performance. IEEE Transactions on Electron Devices, 2015, 62, 3938-3944.	3.0	22
2	Evaluating Chip-Level Impact of Cu/Low- <inline-formula> <tex-math notation="LaTeX">\$kappa \$ </tex-math </inline-formula> Performance Degradation on Circuit Performance at Future Technology Nodes. IEEE Transactions on Electron Devices, 2015, 62, 940-946.	3.0	12
3	Technology/Circuit/System Co-Optimization and Benchmarking for Multilayer Graphene Interconnects at Sub-10-nm Technology Node. IEEE Transactions on Electron Devices, 2015, 62, 1530-1536.	3.0	18
4	Impact of size effects in local interconnects for future technology nodes: A study based on full-chip layouts. , 2014, , .		23
5	System-level optimization and benchmarking for InAs nanowire based gate-all-around tunneling FETs. , 2013, , .		1
6	Cu Interconnect Limitations and Opportunities for SWNT Interconnects at the End of the Roadmap. IEEE Transactions on Electron Devices, 2013, 60, 374-382.	3.0	119
7	Cu/Low-\$k\$ Interconnect Technology Design and Benchmarking for Future Technology Nodes. IEEE Transactions on Electron Devices, 2013, 60, 4041-4047.	3.0	10
8	System-level design and performance modeling for multilevel interconnect networks for carbon nanotube field-effect transistors. , 2012, , .		1
9	Multilevel interconnect networks for the end of the roadmap: Conventional Cu/low-k and emerging carbon based interconnects. , 2011, , .		2