

# Hossein Aghababa

## List of Publications by Year in descending order

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Version: 2024-02-01

24  
papers

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citations

1478505

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1720034

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g-index

24  
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docs citations

24  
times ranked

83  
citing authors

#	ARTICLE	IF	CITATIONS
1	Asymmetric Bidirectional Controlled Quantum Teleportation Using Eight Qubit Cluster State. International Journal of Theoretical Physics, 2022, 61, 1.	1.2	23
2	Bidirectional Quantum Teleportation of an Arbitrary Number of Qubits by Using Four Qubit Cluster State. International Journal of Theoretical Physics, 2021, 60, 378-386.	1.2	19
3	n-Bit Quantum Secret Sharing Protocol Using Quantum Secure Direct Communication. International Journal of Theoretical Physics, 2021, 60, 3744-3759.	1.2	5
4	Bidirectional quantum teleportation of an arbitrary number of qubits over noisy channel. Quantum Information Processing, 2019, 18, 1.	2.2	34
5	Bidirectional Quantum Teleportation of a Class of n-Qubit States by Using $(2n + 2)$ -Qubit Entangled States as Quantum Channel. International Journal of Theoretical Physics, 2018, 57, 175-183.	1.2	30
6	Application of Quantum Gradient Descent as a Learning Algorithm for Factorization Machines. , 2018, , .		2
7	Bidirectional Teleportation of a Two-Qubit State by Using Eight-Qubit Entangled State as a Quantum Channel. International Journal of Theoretical Physics, 2017, 56, 2101-2112.	1.2	55
8	An aging-aware model for the leakage power of nanoscaled digital integrated circuits in IoT era. , 2017, , .		1
9	Knock signal denoising employing a new time domain method. , 2017, , .		1
10	Analysis of stress effects on timing of nano-scaled CMOS digital integrated circuits. , 2016, , .		1
11	A novel leakage power reduction technique for nano-scaled CMOS digital integrated circuits. , 2016, , .		5
12	Estimation of joint probability density function of delay and leakage power with variable skewness. , 2013, , .		4
13	High-performance low-leakage regions of nano-scaled CMOS digital gates under variations of threshold voltage and mobility. Journal of Zhejiang University: Science C, 2012, 13, 460-471.	0.7	7
14	Effects of device and peripheral parameters on transconductance of silicon nanowire transistors. , 2010, , .		0
15	Joint-PDF of timing and power of nano-scaled CMOS digital gates due to channel length variation. , 2010, , .		0
16	Statistical delay modeling of read operation of SRAMs due to channel length variation. , 2010, , .		0
17	Analytical modeling of read stability metric of SRAM cell in nanoscale era. , 2010, , .		1
18	Multi-walled carbon nanotube impedance. , 2010, , .		4

#	ARTICLE	IF	CITATIONS
19	Design of a two-capacitor sample & hold circuit using a two-stage OTA with hybrid cascode compensation. , 2009, , .		0
20	A robust method to estimate Power and Delay for Digital Integrated Circuits. , 2009, , .		0
21	Static power optimization of a Full-Adder under Front-End of Line systematic variations. , 2009, , .		3
22	A compact current-voltage model for carbon nanotube field effect transistors. , 2008, , .		3
23	Analysis of potential function in cylindrical nanowires. , 2008, , .		0
24	Asynchronous circuits design using quantum-dot cellular automata for molecular computing. , 2008, , .		0