# Alex K Jones

List of Publications by Year
in descending order



| | | | |
|---|---|---|---|
| 66 papers | 727 citations | 933447 10 h-index | 642732 23 g-index |
| 67 all docs | 67 docs citations | 67 times ranked | 688 citing authors |

| # | Article | IF | Citations |
|---|---|---|---|
| 1 | Toward Comprehensive Shifting Fault Tolerance for Domain-Wall Memories With PIETT. IEEE Transactions on Computers, 2023, 72, 1095-1109. | 3.4 | 5 |
| 2 | XDWM: A 2D Domain Wall Memory. IEEE Nanotechnology Magazine, 2022, , 1-1. | 2.0 | 0 |
| 3 | Pinning Fault Mode Modeling for DWM Shifting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3319-3323. | 3.0 | 1 |
| 4 | Brain-inspired Cognition in Next-generation Racetrack Memories. Transactions on Embedded Computing Systems, 2022, 21, 1-28. | 2.9 | 2 |
| 5 | Virtual Coset Coding for Encrypted Non-Volatile Memories with Multi-Level Cells. , 2022, , . | | 1 |
| 6 | A CASTLE With TOWERs for Reliable, Secure Phase-Change Memory. IEEE Transactions on Computers, 2021, 70, 1311-1324. | 3.4 | 1 |
| 7 | Tuning Memory Fault Tolerance on the Edge. , 2021, , . | | 0 |
| 8 | A Novel Transverse Read Technique for Domain-Wall â€œRacetrackâ€•Memories. IEEE Nanotechnology Magazine, 2020, 19, 648-652. | 2.0 | 10 |
| 9 | FLOWER and FaME: A Low Overhead Bit-Level Fault-map and Fault-Tolerance Approach for Deeply Scaled Memories. , 2020, , . | | 8 |
| 10 | Predicting Single Event Effects in DRAM. , 2019, , . | | 0 |
| 11 | Yielding optimized dependability assurance through bit inversion. The Integration VLSI Journal, 2019, 64, 105-113. | 2.1 | 1 |
| 12 | Toward Secure, Reliable, and Energy Efficient Phase-change Main Memory with MACE. , 2019, , . | | 0 |
| 13 | PREMSim: A Resilience Framework for Modeling Traditional and Emerging Memory Reliability. , 2019, , . | | 1 |
| 14 | Enabling Fine-Grain Restricted Coset Coding Through Word-Level Compression for PCM. , 2018, , . | | 10 |
| 15 | Racetrack Queues for Extremely Low-Energy FIFOs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1531-1544. | 3.1 | 7 |
| 16 | Improving Sustainability Through Disturbance Crosstalk Mitigation in Deeply Scaled Phase-change Memory. , 2018, , . | | 2 |
| 17 | Achieving Secure, Reliable, and Sustainable Next Generation Computing Memories. , 2018, , . | | 0 |
| 18 | RETROFIT: Fault-Aware Wear Leveling. IEEE Computer Architecture Letters, 2018, 17, 167-170. | 1.5 | 10 |

| # | Article | IF | Citations |
|---|---|---|---|
| 19 | Data Block Partitioning Methods to Mitigate Stuck-At Faults in Limited Endurance Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2358-2371. | 3.1 | 4 |
| 20 | Counter Advance for Reliable Encryption in Phase Change Memory. IEEE Computer Architecture Letters, 2018, 17, 209-212. | 1.5 | 10 |
| 21 | Counter-Based Tree Structure for Row Hammering Mitigation in DRAM. IEEE Computer Architecture Letters, 2017, 16, 18-21. | 1.5 | 39 |
| 22 | Yoda: Judge Me by My Size, Do You?. , 2017, , . | | 10 |
| 23 | Holistic energy efficient crosstalk mitigation in DRAM. , 2017, , . | | 3 |
| 24 | Sustainable fault management and error correction for next-generation main memories. , 2017, , . | | 11 |
| 25 | Dynamic partitioning to mitigate stuck-at faults in emerging memories. , 2017, , . | | 15 |
| 26 | Modeling STT-RAM fabrication cost and impacts in NVSim. , 2016, , . | | 7 |
| 27 | Towards a commodity solution for the internet of things. Computers and Electrical Engineering, 2016, 52, 138-156. | 4.8 | 5 |
| 28 | FusedCache: A Naturally Inclusive, Racetrack Memory, Dual-Level Private Cache. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 69-82. | 2.4 | 20 |
| 29 | Improving Bit Flip Reduction for Biased and Random Data. IEEE Transactions on Computers, 2016, 65, 3345-3356. | 3.4 | 19 |
| 30 | ContextPreRF: Enhancing the Performance and Energy of GPUs With Nonuniform Register Access. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 343-347. | 3.1 | 13 |
| 31 | Life cycle assessment use in the North American building community: summary of findings from a 2011/2012 survey. International Journal of Life Cycle Assessment, 2015, 20, 318-331. | 4.7 | 32 |
| 32 | Reciprocal abstraction for computer architecture co-simulation. , 2015, , . | | 2 |
| 33 | PRES. , 2015, , . | | 27 |
| 34 | Read Performance: The Newest Barrier in Scaled STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1170-1174. | 3.1 | 28 |
| 35 | Design exploration of racetrack lower-level caches. , 2014, , . | | 21 |
| 36 | Weighted-Tuple Synchronization for Parallel Architecture Simulators. , 2014, , . | | 2 |

| # | Article | IF | Citations |
|---|---|---|---|
| 37 | A Practical Data Classification Framework for Scalable and High Performance Chip-Multiprocessors. IEEE Transactions on Computers, 2014, 63, 2905-2918. | 3.4 | 4 |
| 38 | STD-TLB: A STT-RAM-based dynamically-configurable translation lookaside buffer for GPU architectures. , 2014, , . | | 7 |
| 39 | Dynamic life cycle assessment: framework and application to an institutional building. International Journal of Life Cycle Assessment, 2013, 18, 538-552. | 4.7 | 176 |
| 40 | Ocelot: A wireless sensor network and computing engine with commodity palmtop computers. , 2013, , . | | 3 |
| 41 | Considering fabrication in sustainable computing. , 2013, , . | | 11 |
| 42 | Green computing: A life cycle perspective. , 2013, , . | | 6 |
| 43 | A Materials Life Cycle Assessment of a Net-Zero Energy Building. Energies, 2013, 6, 1125-1141. | 3.1 | 83 |
| 44 | Integrating Indoor environmental quality metrics in a dynamic life cycle assessment framework for buildings. , 2012, , . | | 0 |
| 45 | Utilizing measured energy usage to analyze design phase energy models. , 2012, , . | | 1 |
| 46 | Codesign of NoC and Cache Organization for Reducing Access Latency in Chip Multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2012, 23, 1038-1046. | 5.6 | 11 |
| 47 | Combating Write Penalties Using Software Dispatch for On-Chip MRAM Integration. IEEE Embedded Systems Letters, 2012, 4, 82-85. | 1.9 | 1 |
| 48 | GUEST EDITOR'S NOTE â€" INTERACTION BETWEEN COMPILERS AND COMPUTER ARCHITECTURES. Journal of Circuits, Systems and Computers, 2012, 21, 1202001. | 1.5 | 0 |
| 49 | Déjà Vu Switching for Multiplane NoCs. , 2012, , . | | 19 |
| 50 | Compiler-Assisted Data Distribution and Network Configuration for Chip Multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2012, 23, 2058-2066. | 5.6 | 7 |
| 51 | Industrially inspired just-in-time (JIT) teaching. , 2011, , . | | 0 |
| 52 | An inexpensive, battery powered and portable instrument for the optical detection of pathogens. , 2011, , . | | 0 |
| 53 | Towards improving renewable resource utilization with plug-in electric vehicles. , 2011, , . | | 5 |
| 54 | GUEST EDITOR'S NOTE: LARGE-SCALE PARALLEL PROCESSING. Parallel Processing Letters, 2010, 20, 289-291. | 0.6 | 0 |

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|---|---|---|---|
| 55 | Improving renewable resource utilization through integrated generation management. , 2010, , . | | 2 |
| 56 | An architectural space exploration tool for domain specific reconfigurable computing. , 2010, , . | | 3 |
| 57 | Crucial Issues in Logistic Planning for Electric Vehicle Battery Application Service. , 2010, , . | | 5 |
| 58 | Compiler Techniques for Efficient Communications in Circuit Switched Networks for Multiprocessor Systems. IEEE Transactions on Parallel and Distributed Systems, 2009, 20, 331-345. | 5.6 | 8 |
| 59 | Winning with Pinning in NoC. , 2009, , . | | 13 |
| 60 | SYMBOLIC EXPRESSION ANALYSIS FOR COMPILED COMMUNICATION. Parallel Processing Letters, 2008, 18, 567-587. | 0.6 | 3 |
| 61 | Interconnect Customization for a Coarse-grained Reconfigurable Fabric. , 2007, , . | | 5 |
| 62 | Pipelining Tradeoffs of Massively Parallel SuperCISC Hardware Functions. , 2007, , . | | 0 |
| 63 | Exploring RFID Prototyping in the Virtual Laboratory. , 2007, , . | | 5 |
| 64 | A Field Programmable RFID Tag and Associated Design Flow. , 2006, , . | | 11 |
| 65 | A VLIW Processor With Hardware Functions: Increasing Performance While Reducing Power. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1250-1254. | 2.2 | 8 |
| 66 | A Low-Energy Reconfigurable Fabric for the SuperCISC Architecture. , 2006, , . | | 1 |