

Alex K Jones

List of Publications by Year in descending order

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Version: 2024-02-01

66
papers

727
citations

933447

10
h-index

642732

23
g-index

67
all docs

67
docs citations

67
times ranked

688
citing authors

#	ARTICLE	IF	CITATIONS
1	Dynamic life cycle assessment: framework and application to an institutional building. International Journal of Life Cycle Assessment, 2013, 18, 538-552.	4.7	176
2	A Materials Life Cycle Assessment of a Net-Zero Energy Building. Energies, 2013, 6, 1125-1141.	3.1	83
3	Counter-Based Tree Structure for Row Hammering Mitigation in DRAM. IEEE Computer Architecture Letters, 2017, 16, 18-21.	1.5	39
4	Life cycle assessment use in the North American building community: summary of findings from a 2011/2012 survey. International Journal of Life Cycle Assessment, 2015, 20, 318-331.	4.7	32
5	Read Performance: The Newest Barrier in Scaled STT-RAM. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1170-1174.	3.1	28
6	PRES. , 2015, , .		27
7	Design exploration of racetrack lower-level caches. , 2014, , .		21
8	FusedCache: A Naturally Inclusive, Racetrack Memory, Dual-Level Private Cache. IEEE Transactions on Multi-Scale Computing Systems, 2016, 2, 69-82.	2.4	20
9	Déjà Vu Switching for Multiplane NoCs. , 2012, , .		19
10	Improving Bit Flip Reduction for Biased and Random Data. IEEE Transactions on Computers, 2016, 65, 3345-3356.	3.4	19
11	Dynamic partitioning to mitigate stuck-at faults in emerging memories. , 2017, , .		15
12	Winning with Pinning in NoC. , 2009, , .		13
13	ContextPreRF: Enhancing the Performance and Energy of GPUs With Nonuniform Register Access. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2016, 24, 343-347.	3.1	13
14	A Field Programmable RFID Tag and Associated Design Flow. , 2006, , .		11
15	Codesign of NoC and Cache Organization for Reducing Access Latency in Chip Multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2012, 23, 1038-1046.	5.6	11
16	Considering fabrication in sustainable computing. , 2013, , .		11
17	Sustainable fault management and error correction for next-generation main memories. , 2017, , .		11
18	Yoda: Judge Me by My Size, Do You?. , 2017, , .		10

#	ARTICLE	IF	CITATIONS
19	Enabling Fine-Grain Restricted Coset Coding Through Word-Level Compression for PCM. , 2018, , .		10
20	RETROFIT: Fault-Aware Wear Leveling. IEEE Computer Architecture Letters, 2018, 17, 167-170.	1.5	10
21	Counter Advance for Reliable Encryption in Phase Change Memory. IEEE Computer Architecture Letters, 2018, 17, 209-212.	1.5	10
22	A Novel Transverse Read Technique for Domain-Wall "Racetrack" Memories. IEEE Nanotechnology Magazine, 2020, 19, 648-652.	2.0	10
23	A VLIW Processor With Hardware Functions: Increasing Performance While Reducing Power. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2006, 53, 1250-1254.	2.2	8
24	Compiler Techniques for Efficient Communications in Circuit Switched Networks for Multiprocessor Systems. IEEE Transactions on Parallel and Distributed Systems, 2009, 20, 331-345.	5.6	8
25	FLOWER and FaME: A Low Overhead Bit-Level Fault-map and Fault-Tolerance Approach for Deeply Scaled Memories. , 2020, , .		8
26	Compiler-Assisted Data Distribution and Network Configuration for Chip Multiprocessors. IEEE Transactions on Parallel and Distributed Systems, 2012, 23, 2058-2066.	5.6	7
27	STD-TLB: A STT-RAM-based dynamically-configurable translation lookaside buffer for GPU architectures. , 2014, , .		7
28	Modeling STT-RAM fabrication cost and impacts in NVSim. , 2016, , .		7
29	Racetrack Queues for Extremely Low-Energy FIFOs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1531-1544.	3.1	7
30	Green computing: A life cycle perspective. , 2013, , .		6
31	Interconnect Customization for a Coarse-grained Reconfigurable Fabric. , 2007, , .		5
32	Exploring RFID Prototyping in the Virtual Laboratory. , 2007, , .		5
33	Crucial Issues in Logistic Planning for Electric Vehicle Battery Application Service. , 2010, , .		5
34	Towards improving renewable resource utilization with plug-in electric vehicles. , 2011, , .		5
35	Towards a commodity solution for the internet of things. Computers and Electrical Engineering, 2016, 52, 138-156.	4.8	5
36	Toward Comprehensive Shifting Fault Tolerance for Domain-Wall Memories With PIETT. IEEE Transactions on Computers, 2023, 72, 1095-1109.	3.4	5

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37	A Practical Data Classification Framework for Scalable and High Performance Chip-Multiprocessors. IEEE Transactions on Computers, 2014, 63, 2905-2918.	3.4	4
38	Data Block Partitioning Methods to Mitigate Stuck-At Faults in Limited Endurance Memories. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 2358-2371.	3.1	4
39	SYMBOLIC EXPRESSION ANALYSIS FOR COMPILED COMMUNICATION. Parallel Processing Letters, 2008, 18, 567-587.	0.6	3
40	An architectural space exploration tool for domain specific reconfigurable computing. , 2010, , .		3
41	Ocelot: A wireless sensor network and computing engine with commodity palmtop computers. , 2013, , .		3
42	Holistic energy efficient crosstalk mitigation in DRAM. , 2017, , .		3
43	Improving renewable resource utilization through integrated generation management. , 2010, , .		2
44	Weighted-Tuple Synchronization for Parallel Architecture Simulators. , 2014, , .		2
45	Reciprocal abstraction for computer architecture co-simulation. , 2015, , .		2
46	Improving Sustainability Through Disturbance Crosstalk Mitigation in Deeply Scaled Phase-change Memory. , 2018, , .		2
47	Brain-inspired Cognition in Next-generation Racetrack Memories. Transactions on Embedded Computing Systems, 2022, 21, 1-28.	2.9	2
48	A Low-Energy Reconfigurable Fabric for the SuperCISC Architecture. , 2006, , .		1
49	Utilizing measured energy usage to analyze design phase energy models. , 2012, , .		1
50	Combating Write Penalties Using Software Dispatch for On-Chip MRAM Integration. IEEE Embedded Systems Letters, 2012, 4, 82-85.	1.9	1
51	Yielding optimized dependability assurance through bit inversion. The Integration VLSI Journal, 2019, 64, 105-113.	2.1	1
52	PREMSim: A Resilience Framework for Modeling Traditional and Emerging Memory Reliability. , 2019, , .		1
53	A CASTLE With TOWERs for Reliable, Secure Phase-Change Memory. IEEE Transactions on Computers, 2021, 70, 1311-1324.	3.4	1
54	Pinning Fault Mode Modeling for DWM Shifting. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3319-3323.	3.0	1

#	ARTICLE	IF	CITATIONS
55	Virtual Coset Coding for Encrypted Non-Volatile Memories with Multi-Level Cells. , 2022, , .		1
56	Pipelining Tradeoffs of Massively Parallel SuperCISC Hardware Functions. , 2007, , .		0
57	GUEST EDITOR'S NOTE: LARGE-SCALE PARALLEL PROCESSING. Parallel Processing Letters, 2010, 20, 289-291.	0.6	0
58	Industrially inspired just-in-time (JIT) teaching. , 2011, , .		0
59	An inexpensive, battery powered and portable instrument for the optical detection of pathogens. , 2011, , .		0
60	Integrating Indoor environmental quality metrics in a dynamic life cycle assessment framework for buildings. , 2012, , .		0
61	GUEST EDITOR'S NOTE " INTERACTION BETWEEN COMPILERS AND COMPUTER ARCHITECTURES. Journal of Circuits, Systems and Computers, 2012, 21, 1202001.	1.5	0
62	Achieving Secure, Reliable, and Sustainable Next Generation Computing Memories. , 2018, , .		0
63	Predicting Single Event Effects in DRAM. , 2019, , .		0
64	Toward Secure, Reliable, and Energy Efficient Phase-change Main Memory with MACE. , 2019, , .		0
65	Tuning Memory Fault Tolerance on the Edge. , 2021, , .		0
66	XDWM: A 2D Domain Wall Memory. IEEE Nanotechnology Magazine, 2022, , 1-1.	2.0	0