

# Ye-Dam Kim

## List of Publications by Year in descending order

Source: <https://exaly.com/author-pdf/1195636/publications.pdf>

Version: 2024-02-01

9  
papers

83  
citations

1937685  
4  
h-index

2053705  
5  
g-index

9  
all docs

9  
docs citations

9  
times ranked

72  
citing authors

#	ARTICLE	IF	CITATIONS
1	A Reusable Code-Based SAR ADC Design With CDAC Compiler and Synthesizable Analog Building Blocks. IEEE Transactions on Circuits and Systems II: Express Briefs, 2018, 65, 1904-1908.	3.0	29
2	An 8-Bit 1-GS/s Asynchronous Loop-Unrolled SAR-Flash ADC With Complementary Dynamic Amplifiers in 28-nm CMOS. IEEE Journal of Solid-State Circuits, 2021, 56, 1216-1226.	5.4	16
3	A Single-Supply CDAC-Based Buffer-Embedding SAR ADC With Skip-Reset Scheme Having Inherent Chopping Capability. IEEE Journal of Solid-State Circuits, 2020, 55, 2660-2669.	5.4	9
4	A 40nm CMOS 12b 200MS/s Single-amplifier Dual-residue Pipelined-SAR ADC. , 2019, , .		7
5	A 18.5 nW 12-bit 1-kS/s Reset-Energy Saving SAR ADC for Bio-Signal Acquisition in 0.18- $\mu$ m CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, , 1-11.	5.4	5
6	An 8b 1GS/s 2.55mW SAR-Flash ADC with Complementary Dynamic Amplifiers. , 2020, , .		5
7	A Single-Supply Buffer-Embedding SAR ADC with Skip-Reset having Inherent Chopping Capability. , 2019, , .		5
8	A 4 <sup>th</sup> -Order Continuous-Time Delta-Sigma Modulator With Hybrid Noise-Coupling. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 3635-3639.	3.0	4
9	A 6b 28GS/s Four-channel Time-interleaved Current-Steering DAC with Background Clock Phase Calibration. , 2019, , .		3