Henry Selvaraj

List of Publications by Year in Descending Order

25 papers	223 citations	9 h-index	14 g-index
29 ext. papers	290 ext. citations	2.6 avg, IF	2.79 L-index

#	Paper	IF	Citations
25	Interconnection Networks Efficiency in System-on-Chip Distributed Computing System: Concentrated Mesh and Fat Tree **2017**,		2
24	Improved Genetic Algorithm for Finite-Horizon Optimal Control of Nonlinear Systems **2017**,		1
23	A Survey of High Level Synthesis Languages, Tools, and Compilers for Reconfigurable High Performance Computing. *Advances in Intelligent Systems and Computing*, **2014**, 483-492	0.4	22
22	Fast FPGA-based fault injection tool for embedded processors **2013**,		6
21	Accelerating High Performance Computing Applications: Using CPUs, GPUs, Hybrid CPU/GPU, and FPGAs **2012**,		9
20	Overlay-NoC and H-Phy based computing using modern Chip Multiprocessors **2012**,		2
19	Location of Processor Allocator and Job Scheduler and Its Impact on CMP Performance. *International Journal of Electronics and Telecommunications*, **2012**, 58, 9-14		1
18	Energy characteristic of a processor allocator and a network-on-chip. *International Journal of Applied Mathematics and Computer Science*, **2011**, 21, 385-399	1.7	13
17	Fast and efficient processor allocation algorithm for torus-based chip multiprocessors. *Computers and Electrical Engineering*, **2011**, 37, 91-105	4.3	15
16	Efficient logic controller design **2010**,		4
15	HYBRID APPROACH FOR BRAIN TUMOR SEGMENTATION IN MAGNETIC RESONANCE IMAGES USING CELLULAR NEURAL NETWORKS AND OPTIMIZATION TECHNIQUES. *International Journal of Computational Intelligence and Applications*, **2010**, 09, 17-31	1.2	3
14	Synthesis of Processor Allocator for Torus-Based Chip MultiProcessors **2010**,		8
13	Evaluation Scheme for NoC-based CMP with Integrated Processor Management System. *International Journal of Electronics and Telecommunications*, **2010**, 56, 157-168		10
12	Hardware implementation of processor allocation schemes for mesh-based chip multiprocessors. *Microprocessors and Microsystems*, **2010**, 34, 39-48	2.4	12
11	Processor Allocation Problem for NoC-Based Chip Multiprocessors **2009**,		7
10	Review of Packet Switching Technologies for Future NoC **2008**,		13
9	ITERATION-FREE FRACTAL CODING FOR IMAGE COMPRESSION USING GENETIC ALGORITHM. *International Journal of Computational Intelligence and Applications*, **2008**, 07, 429-446	1.2	2

8	An efficient variable partitioning approach for functional decomposition of circuits. *Journal of Systems Architecture*, **2007**, 53, 53-67	5.5	6
7	Input Variable Partitioning Method for Functional Decomposition of Functions Specified by Large Truth Tables **2007**,		3
6	FUNCTIONAL DECOMPOSITION THE VALUE AND IMPLICATION FOR BOTH NEURAL NETWORKS AND DIGITAL DESIGNING. *International Journal of Computational Intelligence and Applications*, **2006**, 06, 123-138	1.2	6
5	MULTILEVEL SYNTHESIS OF FINITE STATE MACHINES BASED ON SYMBOLIC FUNCTIONAL DECOMPOSITION. *International Journal of Computational Intelligence and Applications*, **2006**, 06, 257-271	1.2	7
4	Scheduling and Partitioning Schemes for Low Power Designs Using Multiple Supply Voltages. *Journal of Supercomputing*, **2006**, 35, 93-113	2.5	
3	An application of functional decomposition in ROM-based FSM implementation in FPGA devices. *Journal of Systems Architecture*, **2005**, 51, 424-434	5.5	44
2	Multiple voltage synthesis scheme for low power design under timing and resource constraints. *Integrated Computer-Aided Engineering*, **2005**, 12, 369-378	5.2	
1	A General Approach to Boolean Function Decomposition and its Application in FPGABased Synthesis. *VLSI Design*, **1995**, 3, 289-300		27