Jeng Gong

List of Publications by Year
in descending order

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36 papers	326 citations	1040056 9 h-index	940533 16 g-index
36 all docs	36 docs citations	36 times ranked	274 citing authors

#	Article	IF	Citations
1	High detectivity InGaN-GaN multiquantum well p-n junction photodiodes. IEEE Journal of Quantum Electronics, 2003, 39, 681-685.	1.9	67
2	A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory. , 2006, , .		55
3	The properties of photo chemical-vapor deposition SiO2 and its application in GaN metal-insulator semiconductor ultraviolet photodetectors. Journal of Electronic Materials, 2003, 32, 395-399.	2.2	27
4	High-Performance 1-$muhbox{m}$ GaN n-MOSFET With MgO/MgOâ€“$hbox{TiO}_{2}$ Stacked Gate Dielectrics. IEEE Electron Device Letters, 2011, 32, 306-308.	3.9	21
5	Reliability and Processing Effects of Bandgap-Engineered SONOS (BE-SONOS) Flash Memory and Study of the Gate-Stack Scaling Capability. IEEE Transactions on Device and Materials Reliability, 2008, 8, 416-425.	2.0	14
6	Electrical Characteristics of $hbox{Al}_{2} hbox{O}_{3}/hbox{TiO}_{2}/hbox{Al}_{2}hbox{O}_{3}$ Nanolaminate MOS Capacitor on p-GaN With Post Metallization Annealing and $(hbox{NH}_{4})_{2}hbox{S}_{X}$ Treatments. IEEE Electron Device Letters, 2009, 30, 907-909.	3.9	14
7	High-Quality $hbox{MgO}/hbox{TiO}_{2}/hbox{MgO}$ Nanolaminates on p-GaN MOS Capacitor. IEEE Electron Device Letters, 2010, 31, 558-560.	3.9	14
8	An Octagonal Dual-Gate Transistor With Enhanced and Adaptable Low-Frequency Noise. IEEE Electron Device Letters, 2011, 32, 9-11.	3.9	14
9	Low-frequency noise properties of dynamic-threshold (DT) MOSFET's. IEEE Electron Device Letters, 1999, 20, 532-534.	3.9	12
10	Reliability and Processing Effects of Bandgap Engineered SONOS (BE-SONOS) Flash Memory. , 2007, , .		11
11	Investigation on the Initial Hot-Carrier Injection in P-LDMOS Transistors With Shallow Trench Isolation Structure. IEEE Transactions on Electron Devices, 2008, 55, 3569-3574.	3.0	9
12	Mechanisms and solutions to gate oxide degradation in flash memory by tunnel-oxide nitridation engineering. IEEE Electron Device Letters, 2005, 26, 363-365.	3.9	8
13	Dimension Dependence of Unusual HCI-Induced Degradation on N-Channel High-Voltage DEMOSFET. IEEE Transactions on Electron Devices, 2013, 60, 1723-1729.	3.0	8
14	Effect of fabrication process on the charge trapping behavior of SiON thin films. Solid-State Electronics, 2006, 50, 1171-1174.	1.4	6
15	The Effect of Self-Heating in LDMOSFET Expansion Regime. IEEE Transactions on Electron Devices, 2012, 59, 3042-3047.	3.0	6
16	Demonstration of a HV BCD technology with LV CMOS process. , 2015, , .		6
17	Improving the Electrostatic Discharge Robustness of a Junction Barrier Schottky Diode Using an Embedded p-n-p BJT. IEEE Electron Device Letters, 2014, 35, 1052-1054.	3.9	5
18	An Automated Permuting Capacitor Device for Calibration of IVDs. IEEE Transactions on Instrumentation and Measurement, 2014, 63, 2271-2278.	4.7	5

#	Article	IF	Citations
19	Ultralow Capacitance Transient Voltage Suppressor Design. IEEE Transactions on Electron Devices, 2016, , 1-5.	3.0	5
20	A 5.7-GHz low-noise amplifier with source-degenerated active inductor. Microwave and Optical Technology Letters, 2009, 51, 1955-1958.	1.4	4
21	A Resist-Protection-Oxide Transistor With Adaptable Low-Frequency Noise for Stochastic Neuromorphic Computation in VLSI. IEEE Electron Device Letters, 2011, 32, 1293-1295.	3.9	3
22	A 60â€GHz threeâ€stage low noise amplifier using 0.15â€Î¼m galliumâ€arsenic pseudomorphic highâ€electron mobility transistor technology. Microwave and Optical Technology Letters, 2012, 54, 329-332.	1.4	3
23	The Conduction Characteristics of a 700 V Lateral Insulated-Gate Bipolar Transistor in a Junction Isolation Technology. IEEE Electron Device Letters, 2015, 36, 929-931.	3.9	3
24	Experimental Results of on-State Resistance Reduction by STI Fingers in LDMOSFET. IEEE Electron Device Letters, 2009, 30, 192-194.	3.9	2
25	The study of threshold voltage extraction of nitride spacer NMOS transistors in early stage hot carrier stress. IEEE Transactions on Electron Devices, 2002, 49, 1488-1490.	3.0	1
26	Design of CMOS T/R switch using high-substrate isolation and RF floated body for 1.9-GHz applications. Microwave and Optical Technology Letters, 2009, 51, 2145-2149.	1.4	1
27	Calibrations of inductive voltage dividers by four-terminal-pair bridge with automated permuting capacitors. , 2012, , .		1
28	Using LV process to design high voltage DDDMOSFET and LDMOSFET with 3-D profile structure. , 2013, , .		1
29	Measurement of the Base Resistance at Active Region of Polyemitter Bjt by Noise Method. , 0, , .		0
30	The Oxide-Trap-Distributed Dependence of Exponent Î³ on 1/f/sup Î³/ Noise in Mosfets Device. , 0, , .		0
31	Base current noise degradation of polysilicon emitter npn bjt during constant-current stress. , 0, , .		0
32	A wideband 27-dBm CMOS T/R switch using stacking architecture, high substrate isolation and RF floated body. International Journal of Electronics, 2009, 96, 989-1003.	1.4	0
33	Response analysis of optically modulated scatterer probes for electromagnetic-field measurement. , 2009, , .		0
34	Design of DC to 10â€GHz broadband CMOS transmit/receive switch circuits. Microwave and Optical Technology Letters, 2010, 52, 322-326.	1.4	0
35	The Study of the Electrothermal Property of High-Voltage Drain-Extended MOSFETs. IEEE Transactions on Electron Devices, 2012, 59, 1149-1154.	3.0	0
36	The high temperature DC characteristics of a high voltage lateral insulated-gate bipolar transistors with NPN anode in junction isolation technology. Solid-State Electronics, 2017, 132, 80-85.	1.4	0