Mustafa Berke Yelten

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/1188313/publications.pdf

Version: 2024-02-01

57	451	1040056	794594
papers	citations	9	19
		h-index	g-index

57	57	57	316
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Holistic Device Modeling: Toward a Unified MOSFET Model Including Variability, Aging, and Extreme Operating Conditions. IEEE Transactions on Circuits and Systems II: Express Briefs, 2022, 69, 2635-2640.	3.0	4
2	A Simulation Tool for Space Applications: RadiSPICE. , 2022, , .		1
3	Responsivity Comparison of Different Photodiode Structures. , 2022, , .		0
4	A switchable DC offset cancellation circuit for time-based degradation correction. Analog Integrated Circuits and Signal Processing, 2021, 106, 485-491.	1.4	2
5	A wide-temperature range (77â€“400ÂK) CMOS low-dropout voltage regulatorÂsystem. Analog Integrated Circuits and Signal Processing, 2021, 106, 501-510.	1.4	3
6	Design and validation of an artificial neural network based on analog circuits. Analog Integrated Circuits and Signal Processing, 2021, 106, 475-483.	1.4	4
7	Monitoring modal shape of miniaturized dynamic structures via laser triangulation and stroboscopy. Microsystem Technologies, 2021, 27, 3751-3756.	2.0	1
8	An ISM-Band Multi-Phase Injection-Locked Ring Oscillator. , 2021, , .		6
9	An Automated Setup for the Characterization of Time-Based Degradation Effects Including the Process Variability in 40-nm CMOS Transistors. IEEE Transactions on Instrumentation and Measurement, 2021, 70, 1-10.	4.7	6
10	Gamma Ray Effects on Organic Light-Emitting Diodes (OLEDs). , 2021, , .		0
11	Ultra Low Power Transimpedance Amplifier Design for Receivers with Large-Area Photodetectors. , 2021, , .		0
12	A High Performance TIA Design in 40 nm CMOS. , 2020, , .		7
13	Experimental and modeling studies of automotive-qualified OLEDs under electrical stress. Microelectronics Reliability, 2020, 111, 113704.	1.7	11
14	Design of a tunable LNA and its variability analysis through surrogate modeling. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2020, 33, e2724.	1.9	10
15	A 180-nm X-Band Cryogenic CMOS LNA. IEEE Microwave and Wireless Components Letters, 2020, 30, 395-398.	3.2	12
16	Reliability Testing of 3D-Printed Polyamide Actuators. IEEE Transactions on Device and Materials Reliability, 2020, 20, 152-156.	2.0	5
17	Modeling of Total Ionizing Dose Degradation on 180-nm n-MOSFETs Using BSIM3. IEEE Transactions on Electron Devices, 2019, 66, 4617-4622.	3.0	15
18	Hysteretic Buck-Boost Converter for Wearable Applications. , 2019, , .		0

#	Article	IF	Citations
19	A Cryogenic LC VCO Utilizing Cryogenic Models of Active Devices. , 2019, , .		6
20	On Chip Reconfigurable CMOS Analog Circuit Design and Automation Against Aging Phenomena. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-22.	2.6	2
21	Variability-aware cryogenic models of mosfets: validation and circuit design. Semiconductor Science and Technology, 2019, 34, 115004.	2.0	4
22	Design of Cryogenic LNAs for High Linearity in Space Applications. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 4619-4627.	5.4	26
23	Comparison of ELTs with different shapes and a regular layout transistor in 180 nm CMOS process. , 2019, , .		1
24	Silver nanowire coated knitted wool fabrics for wearable electronic applications. Journal of Engineered Fibers and Fabrics, 2019, 14, 155892501985622.	1.0	21
25	Radiation tolerance impact of trap density near the drain and source regions of a MOSFET. Nuclear Instruments & Methods in Physics Research B, 2019, 449, 1-5.	1.4	4
26	Design of a LC Voltage-Controlled Oscillator for Space Applications in C-Band. , 2019, , .		2
27	A Cryogenic CMOS Low Dropout Voltage Regulator Design for Space Applications. , 2019, , .		2
28	An Offset Cancellation Set-up for Amplifiers Subject to Aging. , 2019, , .		1
29	Design of An Analog Circuit-Based Artificial Neural Network. , 2019, , .		1
30	Statistical MOSFET Modeling Methodology for Cryogenic Conditions. IEEE Transactions on Electron Devices, 2019, 66, 66-72.	3.0	21
31	Cryogenic DC Characteristics of Low Threshold Voltage (VTH) n-channel MOSFETs. Balkan Journal of Electrical and Computer Engineering, 2019, 7, 362-365.	0.6	2
32	Surrogate modeling and variability analysis of onâ€chip spiral inductors. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2018, 31, e2313.	1.9	5
33	Reliability Testing of 3D-Printed Electromechanical Scanning Devices. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 363-370.	1.2	6
34	A High Speed 180 NM CMOS Cryogenic SAR ADC. , 2018, , .		3
35	Time-dependent dielectric breakdown (TDDB) reliability analysis of CMOS analog and radio frequency (RF) circuits. Analog Integrated Circuits and Signal Processing, 2018, 97, 39-47.	1.4	4
36	A Novel Multiple Membership Function Generator for Fuzzy Logic Systems. , 2018, , .		4

#	Article	IF	Citations
37	Design of Logic Gates by Using a Four-Gate Thin Film Transistor (FG TFT). , 2018, , .		0
38	A Rare Event Based Yield Estimation Methodology for Analog Circuits. , 2018, , .		3
39	Aging signature properties and an efficient signature determination tool for online monitoring. The Integration VLSI Journal, 2017, 58, 496-503.	2.1	0
40	A 0.18 Î¼m CMOS X-Band Low Noise Amplifier for Space Applications. , 2017, , .		5
41	Reliability of 3D-printed dynamic scanners. , 2017, , .		0
42	Review: Analog design methodologies for reliability in nanoscale CMOS circuits. , 2017, , .		14
43	A cryogenic modeling methodology of MOSFET I-V characteristics in BSIM3. , 2017, , .		8
44	A high linearity LNA using 180 nm CMOS technology for S-Band. , 2017, , .		2
45	A heuristic sensitivity analysis technique for high-dimensional systems. , 2016, , .		0
46	Efficient signature selection tool for sense & react systems. , 2016, , .		2
47	Scalable and efficient analog parametric fault identification. , 2013, , .		1
48	Model-Based Variation-Aware Integrated Circuit Design. , 2013, , 171-188.		0
49	Variation-Aware Circuit Macromodeling and Design Based on Surrogate Models. Advances in Intelligent Systems and Computing, 2013, , 255-269.	0.6	0
50	Process mismatch analysis based on reduced-order models. , 2012, , .		2
51	Analog Negative-Bias-Temperature-Instability Monitoring Circuit. IEEE Transactions on Device and Materials Reliability, 2012, 12, 177-179.	2.0	6
52	Demystifying Surrogate Modeling for Circuits and Systems. IEEE Circuits and Systems Magazine, 2012, 12, 45-63.	2.3	133
53	Comparison of modeling techniques in circuit variability analysis. International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, 2012, 25, 288-302.	1.9	9
54	Surrogate-Model-Based Analysis of Analog Circuitsâ€"Part II: Reliability Analysis. IEEE Transactions on Device and Materials Reliability, 2011, 11, 466-473.	2.0	21

#	Article	IF	Citations
55	Surrogate-Model-Based Analysis of Analog Circuitsâ€"Part I: Variability Analysis. IEEE Transactions on Device and Materials Reliability, 2011, 11, 458-465.	2.0	31
56	Theoretical analysis and characterization of the tunable matching networks in low noise amplifiers. , 2009, , .		6
57	A novel design procedure for tunable low noise amplifiers. , 2009, , .		6