JoÃ£o Canas Ferreira

List of Publications by Year
in descending order

71	399	1162367 8	1125271 13
papers	citations	h-index	g-index

75	75	75	319
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An FPGA implementation of a long short-term memory neural network. , 2016, , .		39
2	Support for partial run-time reconfiguration of platform FPGAs. Journal of Systems Architecture, 2006, 52, 709-726.	2.5	26
3	Parallel Implementation on FPGA of Support Vector Machines Using Stochastic Gradient Descent. Electronics (Switzerland), 2019, 8, 631.	1.8	23
4	An FPGA-Oriented Baseband Modulator Architecture for 4G/5G Communication Scenarios. Electronics (Switzerland), 2019, 8, 2.	1.8	20
5	Generation of partial FPGA configurations at run-time. , 2008, , .		16
6	Electric Vehicles On-Board Battery Charger for the Future Smart Grids. IFIP Advances in Information and Communication Technology, 2013, , 351-358.	0.5	16
7	REFLECT: Rendering FPGAs to Multi-core Embedded Computing. , 2011, , 261-289.		14
8	Transparent Trace-Based Binary Acceleration for Reconfigurable HW/SW Systems. IEEE Transactions on Industrial Informatics, 2013, 9, 1625-1634.	7.2	12
9	Parallel Implementation of K-Means Algorithm on FPGA. IEEE Access, 2020, 8, 41071-41084.	2.6	12
10	Evaluation of CGRA architecture for real-time processing of biological signals on wearable devices. , 2017, , .		11
11	A framework for hardware cellular genetic algorithms: An application to spectrum allocation in cognitive radio. , 2013, , .		10
12	Tool to support computer architecture teaching and learning. , 2013, , .		10
13	Reconfigurable FPGA-Based FFT Processor for Cognitive Radio Applications. Lecture Notes in Computer Science, 2016, , 223-232.	1.0	10
14	Dynamically reconfigurable LTE-compliant OFDM modulator for downlink transmission. , 2016, , .		9
15	Improving Performance and Energy Consumption in Embedded Systems via Binary Acceleration: A Survey. ACM Computing Surveys, 2021, 53, 1-36.	16.1	9
16	FPGA-based rectification of stereo images. , 2010, , .		8
17	From Instruction Traces to Specialized Reconfigurable Arrays. , 2011, , .		8
18	A scalable array for Cellular Genetic Algorithms: TSP as case study. , 2012, , .		8

#	Article	IF	Citations
19	Generation of hardware modules for run-time reconfigurable hybrid CPU/FPGA systems. IET Computers and Digital Techniques, 2007, 1, 461.	0.9	7
20	Transparent Runtime Migration of Loop-Based Traces of Processor Instructions to Reconfigurable Processing Units. International Journal of Reconfigurable Computing, 2013, 2013, 1-20.	0.2	7
21	Dynamic Partial Reconfiguration of Customized Single-Row Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2019, 27, 116-125.	2.1	7
22	Transparent Acceleration of Program Execution using Reconfigurable Hardware. , 2015, , .		6
23	Generation of Customized Accelerators for Loop Pipelining of Binary Instruction Traces. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2017, 25, 21-34.	2.1	6
24	Flexible and Dynamically Reconfigurable FPGA-Based FS-FBMC Baseband Modulator. , 2018, , .		6
25	Creation of Partial FPGA Configurations at Run-Time. , 2010, , .		5
26	Smart Platform towards Batteries Analysis Based on Internet-of-Things. Procedia Technology, 2014, 17, 520-527.	1.1	5
27	Reconfigurable NC-OFDM Processor for 5G Communications. , 2015, , .		5
28	Scalable hardware architecture for disparity map computation and object location in real-time. Journal of Real-Time Image Processing, 2016, 11, 473-485.	2.2	5
29	An FPGA array for cellular genetic algorithms: Application to the minimum energy broadcast problem. Microprocessors and Microsystems, 2018, 58, 1-12.	1.8	5
30	A Multifunctional Integrated Circuit Router for Body Area Network Wearable Systems. IEEE/ACM Transactions on Networking, 2020, 28, 1981-1994.	2.6	5
31	Design and Implementation of a Circuit for Mesh Networks with Application in Body Area Networks. , 2012, , .		4
32	Analysis of error detection schemes: Toolchain support and hardware/software implications. , 2012, , .		4
33	A Time Synchronization Circuit with an Average 4.6 ns One-Hop Skew for Wired Wearable Networks. , 2014, , .		4
34	Trace-Based Reconfigurable Acceleration with Data Cache and External Memory Support. , 2014, , .		4
35	Dynamically reconfigurable FFT processor for flexible OFDM baseband processing. , 2016, , .		4
36	FPGA-based implementation of a frequency spreading FBMC-OQAM baseband modulator. , 2017, , .		4

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37	Analysis and Evaluation of anEnergy-Efficient Routing Protocol for WSNsCombining Source Routing and MinimumCost Forwarding. Journal of Mobile Multimedia, 2019, 14, 469-504.	0.9	4
38	Exploiting dynamic reconfiguration of platform FPGAs: implementation issues. , 2006, , .		3
39	FPGA-based real-time disparity computation and object location. , 2010, , .		3
40	A Reconfigurable Architecture for Binary Acceleration of Loops with Memory Accesses. ACM Transactions on Reconfigurable Technology and Systems, 2015, 7, 1-20.	1.9	3
41	A Precise and Hardware-Efficient Time Synchronization Method for Wearable Wired Networks. IEEE Sensors Journal, 2016, 16, 1460-1470.	2.4	3
42	Towards a type 0 hypervisor for dynamic reconfigurable systems. , 2017, , .		3
43	Design and Evaluation of a Low Power CGRA Accelerator for Biomedical Signal Processing. , 2018, , .		3
44	Run-time generation of partial FPGA configurations for subword operations. Microprocessors and Microsystems, 2012, 36, 365-374.	1.8	2
45	Run-time generation of partial FPGA configurations. Journal of Systems Architecture, 2012, 58, 24-37.	2.5	2
46	Design and implementation of hybrid circuit/packet switching for wearable systems. , 2014, , .		2
47	An FPGA Framework for Genetic Algorithms: Solving the Minimum Energy Broadcast Problem. , 2015, , .		2
48	A small fully digital openâ€loop clock and data recovery circuit for wired BANs. International Journal of Circuit Theory and Applications, 2016, 44, 530-548.	1.3	2
49	Optimizing OpenCL Code for Performance on FPGA: k-Means Case Study With Integer Data Sets. IEEE Access, 2020, 8, 152286-152304.	2.6	2
50	A Binary Translation Framework for Automated Hardware Generation. IEEE Micro, 2021, 41, 15-23.	1.8	2
51	Architecture for Transparent Binary Acceleration of Loops with Memory Accesses. Lecture Notes in Computer Science, 2013, , 122-133.	1.0	2
52	E-Legging for Monitoring the Human Locomotion Patterns. Journal of Textile Engineering, 2013, 59, 153-158.	0.5	2
53	A time synchronization circuit with sub-microsecond skew for multi-hop wired wearable networks. Microprocessors and Microsystems, 2015, 39, 1029-1038.	1.8	1
54	A Dynamically Reconfigurable Dual-Waveform Baseband Modulator for Flexible Wireless Communications. Journal of Signal Processing Systems, 2020, 92, 409-424.	1.4	1

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55	The REFLECT Design-Flow. , 2013, , 13-34.		1
56	A Parallel-Pipelined OFDM Baseband Modulator with Dynamic Frequency Scaling for 5G Systems. Lecture Notes in Computer Science, 2018, , 511-522.	1.0	1
57	A Reconfigurable Custom Machine for Accelerating Cellular Genetic Algorithms. U Porto Journal of Engineering, 2016, 2, 2-13.	0.2	1
58	An IC architecture for board-level mixed-signal test support. , 0, , .		0
59	Mixed hardware/software applications on dynamically reconfigurable hardware. , 0, , .		0
60	Non-rectangular reconfigurable cores for system-on-chip. Proceedings of SPIE, 2009, , .	0.8	0
61	Run-time generation of partial configurations for arithmetic expressions. , 2010, , .		0
62	Erlang Inspired Hardware. , 2010, , .		0
63	Register Transfer Level Workflow for Application and Evaluation of Soft Error Mitigation Techniques. , 2013, , .		0
64	Preface to the Special Issue on Methods, Tools, and Architectures for Signal and Image Processing. Journal of Signal Processing Systems, 2019, 91, 701-702.	1.4	0
65	Flexible Baseband Modulator Architecture for Multi-Waveform 5G Communications. , 2020, , .		0
66	Executing ARMv8 Loop Traces on Reconfigurable Accelerator via Binary Translation Framework. , 2020, , .		0
67	Transparent Control Flow Transfer between CPU and Accelerators for HPC. Electronics (Switzerland), 2021, 10, 406.	1.8	0
68	A Development Support System for Applications That Use Dynamically Reconfigurable Hardware. Lecture Notes in Computer Science, 2004, , 886-890.	1.0	0
69	Wearable monitoring system for locomotion rehabilitation. , 2013, , 293-298.		0
70	On the Performance Effect of Loop Trace Window Size on Scheduling for Configurable Coarse Grain Loop Accelerators. , 2021, , .		0
71	Hardware architecture for integrate-and-fire signal reconstruction on FPGA. , 2020, , .		0