Jiun-In Guo

List of Publications by Year
in descending order

71	841	759233 12	713466 21
papers	citations	h-index	g-index

71	71	71	327
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A single-camera high dynamic range technique by using contrast enhancement and exposure control. , 2014, , .		0
2	A two level mode decision algorithm for H.264 high profile intra encoding. , 2012, , .		2
3	A 0.5V 25Mpixels/s SVGA 30fps H.264 video decoder chip. , 2011, , .		1
4	Low complexity 3D depth map generation for stereo applications. , 2011, , .		7
5	A low-complexity image stitching algorithm suitable for embedded systems. , 2011, , .		6
6	Multi-core software/hardware co-debug platform with ARM CoreSight™, on-chip test architecture and AXI/AHB bus monitor. , 2011, , .		5
7	Design of Subthreshold SRAMs for Energy-Efficient Quality-Scalable Video Applications. IEEE Journal on Emerging and Selected Topics in Circuits and Systems, 2011, 1, 183-192.	3.6	22
8	A dynamic quality-adjustable H.264 intra coder. IEEE Transactions on Consumer Electronics, 2011, 57, 1203-1211.	3.6	9
9	Dynamic voltage domain assignment technique for low power performance manageable cell based design. , 2010, , .		0
10	A clock-controlled self-stabilized voltage technique with high dynamic power reduction for portable multimedia applications. , 2010, , .		0
11	A BU-based rate control design for H.264 and AVS video coding with ROI support. , 2010, , .		0
12	Efficient IR drop analysis and alleviation methodologies using dual threshold voltages with gate resizing techniques. , 2010, , .		1
13	Low complexity fractional motion estimation with adaptive mode selection for H.264/AVC. , 2010, , .		9
14	Low compute complexity BU-based rate control algorithm for H.264/AVC encoder. , 2010, , .		1
15	A system architecture exploration on the configurable HW/SW co-design for H.264 video decoder. , 2009, , .		8
16	A 252Kgates/4.9Kbytes SRAM/71mW multistandard video decoder for high definition video applications. ACM Transactions on Design Automation of Electronic Systems, 2009, 14, 1-17.	2.6	5
17	A high throughput deblocking filter design supporting multiple video coding standards. , 2009, , .		7
18	High-Throughput H.264/AVC High-Profile CABAC Decoder for HDTV Applications. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1395-1399.	8.3	25

#	Article	IF	Citations
19	A Low Complexity Error Concealment Method for H.264 Video Coding Facilitating Hardware Realization. , 2009, , .		0
20	VisoMT: A Collaborative Multithreading Multicore Processor for Multimedia Applications With a Fast Data Switching Mechanism. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1633-1645.	8.3	5
21	Optimization of VC-1/H.264/AVS Video Decoders on Embedded Processors. , 2009, , .		4
22	CKVdd: A self-stabilization ramp-Vdd Technique for dynamic power reduction. , 2009, , .		0
23	Optimization of AVS-M Video Decoder for Real-time Implementation on Embedded RISC Processors. , 2009, , .		2
24	A Dynamic Quality-Adjustable H.264 Video Encoder for Power-Aware Video Applications. IEEE Transactions on Circuits and Systems for Video Technology, 2009, 19, 1739-1754.	8.3	31
25	A high throughput in-loop de-blocking filter supporting H.264/AVC BP/MP/HP video coding. , 2008, , .		7
26	Joint algorithm/code-level optimization of H.264 video decoder for mobile multimedia applications. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	3
27	A multi-mode entropy decoder with a generic table partition strategy. , 2008, , .		1
28	A novel basic unit level rate control algorithm and architecture for H.264/AVC video encoders. , 2008, , .		0
29	A H.264 basic-unit level rate control algorithm facilitating hardware realization. Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing, 2008, , .	1.8	6
30	A Low Latency Memory Controller for Video Coding Systems. , 2007, , .		6
31	A 160K Gates/4.5 KB SRAM H.264 Video Decoder for HDTV Applications. IEEE Journal of Solid-State Circuits, 2007, 42, 170-182.	5.4	53
32	Low Complexity Multi-Standard Video Player for Portable Multimedia Applications. , 2007, , .		1
33	A Quality Scalable H.264/AVC Baseline Intra Encoder for High Definition Video Applicaitons. Signal Processing Systems Design and Implementation (siPS), IEEE Workshop on, 2007, , .	0.0	5
34	A Versatile Multimedia Functional Unit Design Using the Spurious Power Suppression Technique. , 2006, , .		12
35	A Low Complexity High Quality Interger Motion Estimation Architecture Design for H.264/AVC. , 2006, , .		6
36	Collaborative Multithreading: An Open Scalable Processor Architecture for Embedded Multimedia Applications. , 2006, , .		1

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37	Low Complexity High Quality Fractional Motion Estimation Algorithm and Architecture Design for H.264/AVC. , 2006, , .		12
38	A high-performance direct 2-D transform coding IP design for MPEG-4AVC/H.264. IEEE Transactions on Circuits and Systems for Video Technology, 2006, 16, 472-483.	8.3	41
39	A High Throughput VLSI Architecture Design for H.264 Context-Based Adaptive Binary Arithmetic Decoding with Look Ahead Parsing. , 2006, , .		14
40	A Condition-based Intra Prediction Algorithm for H.264/AVC. , 2006, , .		11
41	An energy-aware IP core design for the variable-length DCT/IDCT targeting at MPEG4 shape-adaptive transforms. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 704-715.	8.3	12
42	A memory-efficient realization of cyclic convolution and its application to discrete cosine transform. IEEE Transactions on Circuits and Systems for Video Technology, 2005, 15, 445-453.	8.3	39
43	Design Exploration of a Spurious Power Suppression Technique (SPST) and Its Applications. , 2005, , .		7
44	An Efficient 2-D DCT/IDCT Core Design Using Cyclic Convolution and Adder-Based Realization. IEEE Transactions on Circuits and Systems for Video Technology, 2004, 14, 416-428.	8.3	32
45	An Efficient IDCT Processor Design for HDTV Applications. Journal of Signal Processing Systems, 2003, 33, 147-155.	1.0	4
46	A LOW-POWER PARAMETERIZED HARDWARE DESIGN FOR THE ONE-DIMENSIONAL DISCRETE FOURIER TRANSFORM OF VARIABLE LENGTHS. Journal of Circuits, Systems and Computers, 2002, 11, 405-426.	1.5	1
47	A generalized architecture for the one-dimensional discrete cosine and sine transforms. IEEE Transactions on Circuits and Systems for Video Technology, 2001, 11, 874-881.	8.3	21
48	Hardware-efficient DFT designs with cyclic convolution and subexpression sharing. IEEE Transactions on Circuits and Systems Part 2: Express Briefs, 2000, 47, 886-892.	2.2	28
49	An efficient design for one-dimensional discrete Hartley transform using parallel additions. IEEE Transactions on Signal Processing, 2000, 48, 2806-2813.	5.3	17
50	A new k-winners-take-all neural network and its array architecture. IEEE Transactions on Neural Networks, 1998, 9, 901-912.	4.2	48
51	A New Array Architecture for Prime-Length Discrete Cosine Transform. IEEE Transactions on Signal Processing, 1993, 41, 436.	5.3	52
52	A new image encryption algorithm and its VLSI architecture. , 0, , .		28
53	An efficient design for one dimensional discrete cosine transform using parallel adders. , 0, , .		0
54	A new chaotic key-based design for image encryption and decryption. , 0, , .		91

#	Article	IF	Citations
55	A low cost 2-D inverse discrete cosine transform design for image compression. , 0, , .		3
56	A new DA-based array for one dimensional discrete Hartley transform. , 0, , .		4
57	A new group distributed arithmetic design for the one dimensional discrete Fourier transform. , 0, , .		6
58	A new hardware efficient design for the one dimensional discrete Fourier transform. , 0, , .		2
59	A new 2-D 8Ã—8 DCT/IDT core design using group distributed arithmetic. , 0, , .		1
60	A parameterized low power design for the variable-length discrete Fourier transform using dynamic pipelining. , 0, , .		0
61	A power-aware SNR-progressive DCT/IDCT IP core design for multimedia transform coding. , 0, , .		2
62	A power-aware IP core design for the variable-length DCT/IDCT targeting at MPEG4 shape-adaptive transforms. , 0, , .		8
63	A high-performance MPEG4 bitstream processing core. , 0, , .		2
64	A power-aware IP core generator for the one-dimensional discrete Fourier transform. , 0, , .		1
65	A parameterized power-aware IP core generator for the 2-D 8Ã—8 DCT/IDCT. , 0, , .		2
66	Reconfigurable low power MPEG-4 texture decoder IP design. , 0, , .		2
67	A high-performance low power direct 2-D transform coding IP design for MPEG-4 AVC/H.264 with a switching power suppression technique. , 0, , .		13
68	A Low-power Motion Compensation IP Core Design for MPEG-1/2/4 Video Decoding. , 0, , .		5
69	A Novel Low-Cost High-Performance VLSI Architecture for MPEG-4 AVC/H.264 CAVLC Decoding. , 0, , .		59
70	An Efficient Direct 2-D Transform Coding IP Design for MPEG-4 AVC/H.264. , 0, , .		12
71	Low Complexity Architecture Design of H.264 Predictive Pixel Compensator for HDTV Application. , 0, , .		10