Doug Burger

List of Publications by Year in descending order

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25 papers	5,943 citations	1040056 9 h-index	1281871 11 g-index
25 all docs	25 docs citations	25 times ranked	2285 citing authors

#	Article	IF	Citations
1	General-purpose code acceleration with limited-precision analog computation. Computer Architecture News, 2014, 42, 505-516.	2.5	63
2	Architecture support for disciplined approximate programming. , 2012, , .		270
3	Neural Acceleration for General-Purpose Approximate Programs. , 2012, , .		484
4	Exploiting microarchitectural redundancy for defect tolerance. , 2012, , .		54
5	Dark silicon and the end of multicore scaling. , 2011, , .		692
6	Dynamically replicated memory. Computer Architecture News, 2010, 38, 3-14.	2.5	33
7	Use ECP, not ECC, for hard failures in resistive memories. Computer Architecture News, 2010, 38, 141-152.	2.5	77
8	Dynamically replicated memory. , 2010, , .		124
9	Better I/O through byte-addressable, persistent memory. , 2009, , .		638
10	Mixed-Signal Approximate Computation: A Neural Predictor Case Study. IEEE Micro, 2009, 29, 104-115.	1.8	9
11	Architecting phase change memory as a scalable dram alternative. , 2009, , .		978
12	Counting Dependence Predictors. , 2008, , .		7
13	A NUCA Substrate for Flexible CMP Cache Sharing. IEEE Transactions on Parallel and Distributed Systems, 2007, 18, 1028-1040.	5.6	111
14	Late-binding. Computer Architecture News, 2007, 35, 347-357.	2.5	3
15	Implementation and Evaluation of a Dynamically Routed Processor Operand Network. , 2007, , .		41
16	Composable Lightweight Processors. , 2007, , .		92
17	Composable Lightweight Processors. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2007, , .	0.0	0
18	Dataflow Predication. , 2006, , .		26

#	Article	IF	Citations
19	Implementation and Evaluation of On-Chip Network Architectures. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	99
20	Distributed Microarchitectural Protocols in the TRIPS Prototype Processor. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	112
21	Design and Implementation of the TRIPS Primary Memory System. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	8
22	Merging Head and Tail Duplication for Convergent Hyperblock Formation. , 2006, , .		14
23	Measuring Experimental Error in Microprocessor Simulation. , 2001, , .		106
24	Efficient synchronization. Computer Architecture News, 1997, 25, 170-180.	2.5	24
25	The SimpleScalar tool set, version 2.0. Computer Architecture News, 1997, 25, 13-25.	2.5	1,878