Nithin Kumar Y B

List of Publications by Year
in descending order

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27 papers	192 citations	1478505 6 h-index	1281871 11 g-index
27 all docs	27 docs citations	27 times ranked	107 citing authors

#	Article	IF	Citations
1	A 1-V, 3-GHz Strong-Arm Latch Voltage Comparator for High Speed Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2918-2922.	3.0	26
2	Approximate radix-8 Booth multiplier for low power and high speed applications. Microelectronics Journal, 2020, 101, 104816.	2.0	20
3	Design of Approximate Booth Squarer for Error-Tolerant Computing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 1230-1241.	3.1	18
4	Device and circuit level performance analysis of novel InAs/Si heterojunction double gate tunnel field effect transistor. Superlattices and Microstructures, 2016, 94, 119-130.	3.1	17
5	Reversible full/half adder with optimum power dissipation. , 2016, , .		12
6	A 1.2 V, Highly Reliable RHBD 10T SRAM Cell for Aerospace Application. IEEE Transactions on Electron Devices, 2021, 68, 2265-2270.	3.0	12
7	A fine grained position for modular core on NoC. , 2015, , .		11
8	Design and Implementation of Reversible Logic based RGB to Gray scale Color Space Converter. , 2018, , .		10
9	Low power, high speed error tolerant multiplier using approximate adders. , 2015, , .		8
10	Training of Generative Adversarial Networks with Hybrid Evolutionary Optimization Technique. , 2019, , .		8
11	An Approximate Low-Power Lifting Scheme Using Reversible Logic. IEEE Access, 2020, 8, 183367-183377.	4.2	8
12	Inexact Signed Wallace Tree Multiplier Design Using Reversible Logic. IEEE Access, 2021, 9, 108119-108130.	4.2	8
13	Quantization aware approximate multiplier and hardware accelerator for edge computing of deep learning applications. The Integration VLSI Journal, 2021, 81, 268-279.	2.1	6
14	Characterization of a Novel Low Leakage Power and Area Efficient 7T SRAM Cell. , 2016, , .		5
15	6.25â€…GHz, 1â€…mV input resolution auxiliary circuit assisted comparator in 65â€‰nm CMOS process. IET Circuits, Devices and Systems, 2020, 14, 340-346.	1.4	5
16	A Novel Complex Filter Design With Dual Feedback for High Frequency Wireless Receiver Applications. IEEE Transactions on Circuits and Systems II: Express Briefs, 2021, 68, 1748-1752.	3.0	4
17	A Novel Single Event Upset Tolerant 12T Memory Cell for Aerospace Applications. , 2020, , .		3
18	A Low-Power Auxiliary Circuit for Level-Crossing ADCs in IoT-Sensor Applications. , 2018, , .		2

#	Article	IF	Citations
19	An Asynchronous Analog to Digital Converter for Video Camera Applications. , 2019, , .		2
20	Generation of complex impedance for complex filter design using fully balanced current conveyors. Analog Integrated Circuits and Signal Processing, 2020, 105, 203-214.	1.4	2
21	A novel tunable bandgap voltage and current reference generation circuit. Analog Integrated Circuits and Signal Processing, 2021, 107, 331-338.	1.4	2
22	Design and Analysis of Approximate Multipliers for Error-Tolerant Applications. , 2018, , .		1
23	$$pm , 0.5$$ÂV, 254Â$$upmu $$W Second-Order Tunable Biquad Low-Pass Filter with 7.3ÂfJ FOM Using a Novel Low-Voltage Fully Balanced Current-Mode Circuit. Circuits, Systems, and Signal Processing, 2021, 40, 2114-2134.	2.0	1
24	A 1-V, 10-bit, 250 MS/s, Current-Steering Segmented DAC for Video Applications. , 2021, , .		1
25	Design of Area-Power-Delay Efficient Square Root Carry Select Adder. , 2018, , .		0
26	A 1-V, 5-Bit, 180-ÂµW, Differential Pulse Position Modulation ADC in 65-nm CMOS Process. , 2021, , .		0
27	A 1.8 V Quadrature Phase LC Oscillator for 5G Applications. , 2020, , .		0