Christopher L Ayala

List of Publications by Year
in descending order

23	391	687363 13	888059 17
papers	citations	h-index	g-index

23	23	23	150
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 16-Bit Parallel Prefix Carry Look-Ahead Kogge-Stone Adder Implemented in Adiabatic Quantum-Flux-Parametron Logic. IEICE Transactions on Electronics, 2022, E105.C, 270-276.	0.6	4
2	Adiabatic Quantum-Flux-Parametron: A Tutorial Review. IEICE Transactions on Electronics, 2022, E105.C, 251-263.	0.6	17
3	MANA: A Monolithic Adiabatic iNtegration Architecture Microprocessor Using 1.4-zJ/op Unshunted Superconductor Josephson Junction Devices. IEEE Journal of Solid-State Circuits, 2021, 56, 1152-1165.	5.4	49
4	Buffer Reduction Via N-Phase Clocking in Adiabatic Quantum-Flux-Parametron Benchmark Circuits. IEEE Transactions on Applied Superconductivity, 2021, 31, 1-8.	1.7	8
5	A semi-custom design methodology and environment for implementing superconductor adiabatic quantum-flux-parametron microprocessors. Superconductor Science and Technology, 2020, 33, 054006.	3.5	22
6	A compact AQFP logic cell design using an 8-metal layer superconductor process. Superconductor Science and Technology, 2020, 33, 035010.	3.5	16
7	Fabrication of Adiabatic Quantum-Flux-Parametron Integrated Circuits Using an Automatic Placement Tool Based on Genetic Algorithms. IEEE Transactions on Applied Superconductivity, 2019, 29, 1-6.	1.7	14
8	An adiabatic superconductor 8-bit adder with 24kBT energy dissipation per junction. Applied Physics Letters, 2019, 114, .	3.3	47
9	AQFPTX: Adiabatic Quantum-Flux-Parametron Timing eXtraction Tool. , 2019, , .		10
10	Design and Implementation of a 16-Word by 1-Bit Register File Using Adiabatic Quantum Flux Parametron Logic. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-4.	1.7	25
11	Synthesis Flow for Cell-Based Adiabatic Quantum-Flux-Parametron Structural Circuit Generation With HDL Back-End Verification. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-5.	1.7	25
12	Majority-Logic-Optimized Parallel Prefix Carry Look-Ahead Adder Families Using Adiabatic Quantum-Flux-Parametron Logic. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-7.	1.7	28
13	Development and Demonstration of Routing and Placement EDA Tools for Large-Scale Adiabatic Quantum-Flux-Parametron Circuits. IEEE Transactions on Applied Superconductivity, 2017, 27, 1-9.	1.7	23
14	HDL-Based Modeling Approach for Digital Simulation of Adiabatic Quantum Flux Parametron Logic. IEEE Transactions on Applied Superconductivity, 2016, 26, 1-5.	1.7	25
15	Experimental demonstration of a nanoelectromechanical switch-based logic library including sequential and combinational gates. , 2016, , .		0
16	Experimental demonstration of a nanoelectromechanical switch-based logic library including sequential and combinational gates. , 2016, , .		0
17	Nanoelectromechanical digital logic circuits using curved cantilever switches with amorphous-carbon-coated contacts. Solid-State Electronics, 2015, 113, 157-166.	1.4	10
18	Ultra-low-energy adiabatic dynamic logic circuits using nanoelectromechanical switches. , 2015, , .		2

#	Article	IF	Citations
19	A 6.7 MHz nanoelectromechanical ring oscillator using curved cantilever switches coated with amorphous carbon. , 2014, , .		7
20	Amorphous carbon active contact layer for reliable nanoelectromechanical switches. , 2014, , .		21
21	Analytical Compact Model in Verilog-A for Electrostatically Actuated Ohmic Switches. IEEE Transactions on Electron Devices, 2014, 61, 2186-2194.	3.0	15
22	Electromechanical design space exploration for electrostatically actuated ohmic switches using extended parallel plate compact model. Solid-State Electronics, 2014, 99, 93-100.	1.4	6
23	Data-Flow Microarchitecture for Wide Datapath RSFQ Processors: Design Study. IEEE Transactions on Applied Superconductivity, 2011, 21, 787-791.	1.7	17