Philip Jacob

List of Publications by Year
in descending order

5 papers	108 citations	2258059 3 h-index	2550090 3 g-index
5 all docs	5 docs citations	5 times ranked	109 citing authors

#	Article	IF	Citations
1	Mitigating Memory Wall Effects in High-Clock-Rate and Multicore CMOS 3-D Processor Memory Stacks. Proceedings of the IEEE, 2009, 97, 108-122.	21.3	52
2	A 40 Gs/s Time Interleaved ADC Using SiGe BiCMOS Technology. IEEE Journal of Solid-State Circuits, 2010, 45, 380-390.	5.4	41
3	A 3-D Cache With Ultra-Wide Data Bus for 3-D Processor-Memory Integration. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 967-977.	3.1	15
4	A 3-tier, 3-D FD-SOI SRAM macro. , 2008, , .		0
5	Correction to “A 40 GS/s Time Interleaved ADC Using SiGe BiCMOS Technology”. IEEE Journal of Solid-State Circuits, 2010, 45, 2210-2210.	5.4	0