Gwan Choi

List of Publications by Year
in descending order

31 papers	189 citations	2258059 3 h-index	2272923 4 g-index
31 all docs	31 docs citations	31 times ranked	128 citing authors

#	Article	IF	Citations
1	Overlapped list successive cancellation approach for hardware efficient polar code decoder. , 2016, , .		2
2	MIMO satellite communication with accelerated dual paths asynchronous design. Analog Integrated Circuits and Signal Processing, 2016, 88, 223-231.	1.4	0
3	Compressive sensing and reception for MIMO-OFDM based cognitive radio. , 2015, , .		7
4	Accelerated Dual-Path Asynchronous Circuit. IEEE Transactions on Circuits and Systems II: Express Briefs, 2015, 62, 856-860.	3.0	1
5	Transantral Orbital Floor Fracture Repair Using a Folded Silastic Tube. Clinical and Experimental Otorhinolaryngology, 2015, 8, 250.	2.1	5
6	Risk Factors of Saddle Nose Deformity after Septoplasty. Korean Journal of Otorhinolaryngology-Head and Neck Surgery, 2015, 58, 859.	0.2	0
7	Asynchronous baseband processor design for cooperative MIMO satellite communication. , 2014, , .		5
8	Signal reconstruction processor design for compressive sensing. , 2014, , .		2
9	Asynchronous design for precision-scaleable energy-efficient LDPC decoder. , 2014, , .		0
10	Data processing logic for stacked wafer-scale CMOS radiation sensor network. , 2013, , .		0
11	Support Vector Machine Based Detection of Drowsiness Using Minimum EEG Features. , 2013, , .		28
12	Clinical Usefulness of Otoacoustic Emission Sum in Sudden Sensorineural Hearing Loss Patients. Korean Journal of Otorhinolaryngology-Head and Neck Surgery, 2013, 56, 212.	0.2	0
13	Exploiting path diversity for low-latency and high-bandwidth with the dual-path NoC router. , 2012, , .		3
14	WaveSync: A low-latency source synchronous bypass network-on-chip architecture. , 2012, , .		8
15	Intra-Flit Skew Reduction for Asynchronous Bypass Channel in NoCs. , 2011, , .		5
16	Asynchronous Bypass Channels for Multi-Synchronous NoCs: A Router Microarchitecture, Topology, and Routing Algorithm. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 1663-1676.	2.7	13
17	Asynchronous Bypass Channels: Improving Performance for Multi-synchronous NoCs. , 2010, , .		14
18	Data Handling Limits of On-Chip Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 707-713.	3.1	5

#	Article	IF	Citations
19	Dynamically reconfigurable soft output MIMO detector. , 2008, , .		10
20	Multi-Rate Layered Decoder Architecture for Block LDPC Codes of the IEEE 802.11n Wireless Standard. , 2007, , .		43
21	Minimum-Energy LDPC Decoder for Real-Time Mobile Application. , 2007, , .		4
22	Timing Failure Analysis of Commercial CPUs Under Operating Stress. , 2006, , .		0
23	Information Theoretic Approach to Address Delay and Reliability in Long On-Chip Interconnects. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	0
24	Verification Simulation Acceleration Using Code-Perturbation. Journal of Electronic Testing: Theory and Applications (JETTA), 2000, 16, 83-90.	1.2	1
25	The single event upset characteristics of the 486-DX4 microprocessor. , 0, , .		15
26	Reconfigurable multi-functioning logic structures: a case study of MMX/floating-point unit design. , 0, , .		0
27	Si-emulation: system verification using simulation and emulation. , 0, , .		4
28	Simulation using code-perturbation: black- and white-box approach. , 0, , .		0
29	ECC: extended condition coverage for design verification using excitation and observation. , 0, , .		2
30	An LDPC decoding schedule for memory access reduction. , 0, , .		6
31	Low-Power On-The-Fly Reconfigurable Iterative MIMO Detection and LDPC Decoding Design. Applied Mechanics and Materials, 0, 496-500, 1825-1829.	0.2	6