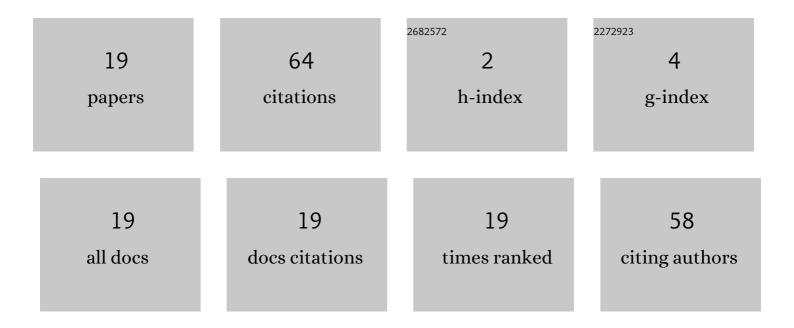
Klaus Hofmann

List of Publications by Year in descending order

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#	Article	IF	CITATIONS
1	Deadlock-free routing algorithms for 3-dimension Networks-on-Chip with reduced vertical channel density topologies. , 2012, , .		11
2	Deadlock-free generic routing algorithms for 3-dimensional Networks-on-Chip with reduced vertical link density topologies. Journal of Systems Architecture, 2013, 59, 528-542.	4.3	8
3	A Scalable Fully Synthesized Phase-to-Digital Converter for Phase and Duty-Cycle Measurement of High-Speed Clocks. , 2018, , .		7
4	A simulation framework for 3-dimension Networks-on-chip with different vertical channel density configurations. , 2012, , .		6
5	Dynamic quadrant partitioning adaptive routing algorithm for irregular reduced vertical link density topology 3-Dimensional Network-on-Chips. , 2014, , .		6
6	Efficient wearable real-time vital signs monitoring system. , 2015, , .		5
7	Highly reliable and power efficient NOC interconnects. , 2011, , .		4
8	Performability measurement of coding algorithms for network on chip. , 2013, , .		3
9	Energy Efficient Synchronous - Asynchronous Circuit-Switched NoC. , 2020, , .		3
10	Tunneling Magnetoresistance DC Current Transformer for Ion Beam Diagnostics. Sensors, 2021, 21, 3043.	3.8	3
11	Performability of error control schemes for NOC interconnects. , 2012, , .		2
12	NoCDepend: A Flexible and Scalable Dependability Technique for 3D Networks-on-Chip. , 2015, , .		2
13	Coding algorithms for network on a chip. , 2013, , .		1
14	Influence of moisture on the electrical properties of solution processed multilayer high-k ZrO ₂ -capacitors. RSC Advances, 2015, 5, 107608-107615.	3.6	1
15	A 2.5 GHz All-Digital Multiphase DLL and Phase Shifter in 65 nm CMOS using a Scalable Phase-to-Digital Converter. , 2019, , .		1
16	Double-Layer Energy Efficient Synchronous-Asynchronous Circuit-Switched NoC. Electronics (Switzerland), 2021, 10, 1821.	3.1	1
17	Hybrid Mesh-Ring wireless NoC for multi-core system. , 2013, , .		0
18	Fast Digital Clock Calibration of a Differential 6.4 Gb/s/pin Bidirectional Asymmetric Memory Interface. IEEE Transactions on Circuits and Systems II: Express Briefs, 2020, 67, 2387-2391.	3.0	0

#	Article	IF	CITATIONS
19	Optimized System-Level Design Methods for NoC-Based Many Core Embedded Systems. Advances in Systems Analysis, Software Engineering, and High Performance Computing Book Series, 2014, , 150-179.	0.5	0