Jiang Hu

List of Publications by Year
in descending order

88	916	567281 15	642732 23
papers	citations	h-index	g-index

88	88	88	466
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Towards Provably-Secure Analog and Mixed-Signal Locking Against Overproduction. IEEE Transactions on Emerging Topics in Computing, 2022, 10, 386-403.	4.6	4
2	Design Rule Violation Prediction at Sub-10-nm Process Nodes Using Customized Convolutional Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 3503-3514.	2.7	1
3	Double Deep Q-Learning Based Irrigation and Chemigation Control. , 2022, , .		0
4	Deep Reinforcement Learning-Based Irrigation Scheduling. Transactions of the ASABE, 2020, 63, 549-556.	1.1	15
5	Breaking Analog Locking Techniques. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2157-2170.	3.1	11
6	Exploring a Machine Learning Approach to Performance Driven Analog IC Placement. , 2020, , .		13
7	Scaled Population Arithmetic for Efficient Stochastic Computing. , 2020, , .		5
8	Enhancing Generalization of Wafer Defect Detection by Data Discrepancy-aware Preprocessing and Contrast-varied Augmentation. , 2020, , .		0
9	EffiTest2: Efficient Delay Test and Prediction for Post-Silicon Clock Skew Configuration Under Process Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 705-718.	2.7	12
10	Improving QoS for Global Dual-Criticality Scheduling on Multiprocessors. , 2019, , .		4
11	Dynamic Approximation of JPEG Hardware. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2019, 38, 295-308.	2.7	1
12	A Built-In Self-Test and <italic>In Situ</italic> Analog Circuit Optimization Platform. IEEE Transactions on Circuits and Systems I: Regular Papers, 2018, 65, 3445-3458.	5.4	24
13	A Simple Yet Efficient Accuracy-Configurable Adder Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2018, 26, 1112-1125.	3.1	51
14	Using Imprecise Computing for Improved Non-Preemptive Real-Time Scheduling. , 2018, , .		2
15	Routing perturbation for enhanced security in split manufacturing. , 2017, , .		18
16	A simple yet efficient accuracy configurable adder design. , 2017, , .		5
17	Thwarting analog IC piracy via combinational locking. , 2017, , .		38
18	Making split fabrication synergistically secure and manufacturable. , 2017, , .		6

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19	Reinforcement Learning Control for Water-Efficient Agricultural Irrigation. , 2017, , .		20
20	A Reliable Soil Moisture Sensing Methodology for Agricultural Irrigation. , 2017, , .		3
21	Front-end-of-line attacks in split manufacturing. , 2017, , .		6
22	Making split fabrication synergistically secure and manufacturable. , 2017, , .		2
23	A comparative study on neural network-based prediction of smart community energy consumption. , 2017, , .		2
24	GPU acceleration for Bayesian control of Markovian genetic regulatory networks. , 2016, , .		3
25	GPU acceleration for PCA-based statistical static timing analysis. , 2015, , .		4
26	Built-In Self Optimization for Variation Resilience of Analog Filters. , 2015, , .		9
27	Guest Editorial: Special Section on Physical Design Techniques for Advanced Technology Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 501-501.	2.7	1
28	Having your cake and eating it too: Energy savings without performance loss through resource sharing driven power management. , 2015, , .		6
29	Proximity Sensing Based on a Dynamic Vision Sensor for Mobile Devices. IEEE Transactions on Industrial Electronics, 2015, 62, 536-544.	7.9	26
30	STORM: A Simple Traffic-Optimized Router Microarchitecture for Networks-on-Chip. , 2014, , .		1
31	Boostable Repeater Design for Variation Resilience in VLSI Interconnects. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1619-1631.	3.1	3
32	Resource allocation algorithms for guaranteed service in application-specific NoCs. , 2013, , .		1
33	Dual-Level Adaptive Supply Voltage System for Variation Resilience. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1041-1052.	3.1	4
34	A low overhead built-in delay testing with voltage and frequency adaptation for variation resilience. , 2012, , .		1
35	In-network Monitoring and Control Policy for DVFS of CMP Networks-on-Chip and Last Level Caches. , 2012, , .		30
36	Guest Editorial Special Section on the 2011 International Symposium on Physical Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2012, 31, 165-166.	2.7	0

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37	Simultaneous Technology Mapping and Placement for Delay Minimization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 416-426.	2.7	3
38	Physical design techniques for optimizing RTA-induced variations. , 2010, , .		0
39	Combinatorial Algorithms for Fast Clock Mesh Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 131-141.	3.1	25
40	Pattern Sensitive Placement Perturbation for Manufacturability. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1002-1006.	3.1	5
41	An Effective Gated Clock Tree Design Based on Activity and Register Aware Placement. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1639-1648.	3.1	30
42	A New Algorithm for Simultaneous Gate Sizing and Threshold Voltage Assignment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 223-234.	2.7	63
43	Scalable Analysis of Mesh-Based Clock Distribution Networks Using Application-Specific Reduced Order Modeling. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1342-1353.	2.7	6
44	Discrete Buffer and Wire Sizing for Link-Based Non-Tree Clock Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 1025-1035.	3.1	18
45	Useful clock skew optimization under a multi-corner multi-mode design framework. , 2010, , .		8
46	A single layer zero skew clock routing in X architecture. Science in China Series F: Information Sciences, 2009, 52, 1466-1475.	1.1	2
47	A fast general slew constrained minimum cost buffering algorithm. Microelectronics Journal, 2009, 40, 1482-1486.	2.0	0
48	Design of Voltage Overscaled Low-Power Trellis Decoders in Presence of Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 439-443.	3.1	7
49	Gate Sizing for Cell-Library-Based Designs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 818-825.	2.7	21
50	Robust Clock Tree Routing in the Presence of Process Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1385-1397.	2.7	16
51	Low power clock buffer planning methodology in F-D placement for large scale circuit design. , 2008, , .		0
52	Gate planning during placement for gated clock network. , 2008, , .		3
53	Planar-CRX: A Single-Layer Zero Skew Clock Routing in X-Architecture. , 2007, , .		1
54	An Exact Jumper-Insertion Algorithm for Antenna Violation Avoidance/Fixing Considering Routing Obstacles. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 719-733.	2.7	5

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55	Fast Algorithms for Slew-Constrained Minimum Cost Buffering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 2009-2022.	2.7	51
56	Modeling, optimization and control of rotary traveling-wave oscillator. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	3
57	Integrated Placement and Skew Optimization for Rotary Clocking. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 149-158.	3.1	8
58	Utilizing Redundancy for Timing Critical Interconnect. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1067-1080.	3.1	3
59	A New Fast Slew Buffering Algorithm Without Input Slew Assumptions. , 2007, , .		1
60	Unified adaptivity optimization of clock and logic signals. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	1
61	A Placement Methodology for Robust Clocking. , 2007, , .		3
62	Wire Sizing and Spacing for Lithographic Printability and Timing Optimization. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 1332-1340.	3.1	2
63	Fast Decap Allocation Based on Algebraic Multigrid. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	2
64	Combinatorial Algorithms for Fast Clock Mesh Optimization. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6
65	Steiner network construction for timing critical nets. Proceedings - Design Automation Conference, 2006, , .	0.0	0
66	Fast algorithms for slew constrained minimum cost buffering. Proceedings - Design Automation Conference, 2006, , .	0.0	0
67	Accurate estimation of global buffer delay within a floorplan. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 1140-1145.	2.7	26
68	Reducing clock skew variability via crosslinks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 1176-1182.	2.7	25
69	Analytical bound for unwanted clock skew due to wire width variation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 1869-1876.	2.7	0
70	Antenna avoidance in layer assignment. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2006, 25, 734-738.	2.7	21
71	Integrated Placement and Skew Optimization for Rotary Clocking. , 2006, , .		19
72	Associative Skew Clock Routing for Difficult Instances. , 2006, , .		2

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73	Navigating registers in placement for clock network minimization. , 2005, , .		36
74	An efficient merging scheme for prescribed skew clock routing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2005, 13, 750-754.	3.1	16
75	Simultaneous Driver Sizing and Buffer Insertion Usinga Delay Penalty Estimation Technique. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 136-141.	2.7	16
76	Porosity-Aware Buffered Steiner Tree Construction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 517-526.	2.7	9
77	A Methodology for the Simultaneous Design of Supply and Signal Networks. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2004, 23, 1614-1624.	2.7	7
78	A practical methodology for early buffer and wire resource allocation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 573-583.	2.7	36
79	Buffer insertion with adaptive blockage avoidance. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2003, 22, 492-498.	2.7	17
80	Buffered clock tree for high quality IC design. , 0, , .		34
81	Exploiting level sensitive latches in wire pipelining. , 0, , .		5
82	Layer assignment for crosstalk risk minimization. , 0, , .		0
83	Library cell layout with Alt-PSM compliance and composability. , 0, , .		0
84	DiCER: distributed and cost-effective redundancy for variation tolerance. , 0, , .		1
85	Clock network minimization methodology based on incremental placement. , 0, , .		0
86	Register placement for low power clock network. , 0, , .		5
87	Skew scheduling and clock routing for improved tolerance to process variations. , 0, , .		7
88	High performance clock routing in X-architecture. , 0, , .		9