Eduardo Antonio CÃ©sar Da Costa

List of Publications by Year
in descending order

8 papers	199 citations	1478505 6 h-index	1720034 7 g-index
8 all docs	8 docs citations	8 times ranked	110 citing authors

#	Article	IF	Citations
1	Design of a low power and robust VLSI power line interference canceler with optimized arithmetic operators. Analog Integrated Circuits and Signal Processing, 2022, 112, 247-261.	1.4	1
2	On the Resiliency of NCFET Circuits Against Voltage Over-Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1481-1492.	5.4	16
3	Approximate Pruned and Truncated Haar Discrete Wavelet Transform VLSI Hardware for Energy-Efficient ECG Signal Processing. IEEE Transactions on Circuits and Systems I: Regular Papers, 2021, 68, 1814-1826.	5.4	27
4	A Cross-Layer Gate-Level-to-Application Co-Simulation for Design Space Exploration of Approximate Circuits in HEVC Video Encoders. IEEE Transactions on Circuits and Systems for Video Technology, 2020, 30, 3814-3828.	8.3	29
5	Design Methodology to Explore Hybrid Approximate Adders for Energy-Efficient Image and Video Processing Accelerators. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 2137-2150.	5.4	52
6	Power-, Area-, and Compression-Efficient Eight-Point Approximate 2-D Discrete Tchebichef Transform Hardware Design Combining Truncation Pruning and Efficient Transposition Buffers. IEEE Transactions on Circuits and Systems I: Regular Papers, 2019, 66, 680-693.	5.4	20
7	Power-Efficient Sum of Absolute Differences Hardware Architecture Using Adder Compressors for Integer Motion Estimation Design. IEEE Transactions on Circuits and Systems I: Regular Papers, 2017, 64, 3126-3137.	5.4	53
8	The 4-2 Fused Adderâ€“Subtractor Compressor for Low-Power Butterfly-Based Hardware Architectures. Circuits, Systems, and Signal Processing, 0, , 1.	2.0	1