Xiaoyao Liang

List of Publications by Year
in descending order

26 papers	566 citations	1478505 6 h-index	1199594 12 g-index
26 all docs	26 docs citations	26 times ranked	421 citing authors

#	Article	IF	Citations
1	SoBS-X: Squeeze-Out Bit Sparsity for ReRAM-Crossbar-Based Neural Network Accelerator. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2023, 42, 204-217.	2.7	2
2	Integrated Power Anomaly Defense: Towards Oversubscription-Safe Data Centers. IEEE Transactions on Cloud Computing, 2022, 10, 1875-1887.	4.4	3
3	Quantitative analysis of abnormalities in gynecologic cytopathology with deep learning. Laboratory Investigation, 2021, 101, 513-524.	3.7	7
4	Fast Tumor Detector in Whole-Slide Image With Dynamic Programing Based Monte Carlo Sampling. , 2020, , .		3
5	A Prediction Model of Microsatellite Status from Histology Images. , 2020, , .		6
6	IBOM: An Integrated and Balanced On-Chip Memory for High Performance GPGPUs. IEEE Transactions on Parallel and Distributed Systems, 2018, 29, 586-599.	5.6	4
7	In-growth test for monolithic 3D integrated SRAM. , 2018, , .		3
8	Sneak-Path Based Test and Diagnosis for 1R RRAM Crossbar Using Voltage Bias Technique. , 2017, , .		17
9	Fault clustering technique for 3D memory BISR. , 2017, , .		2
10	Power Attack Defense: Securing Battery-Backed Data Centers. , 2016, , .		12
11	A Learning Algorithm for Bayesian Networks and Its Efficient Implementation on GPUs. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 17-30.	5.6	5
12	Energy-Efficient eDRAM-Based On-Chip Storage Architecture for GPGPUs. IEEE Transactions on Computers, 2016, 65, 122-135.	3.4	20
13	Exploring Hardware Profile-Guided Green Datacenter Scheduling. , 2015, , .		4
14	Efficient graph computation on hybrid CPU and GPU systems. Journal of Supercomputing, 2015, 71, 1563-1586.	3.6	22
15	Buddy SM. Transactions on Architecture and Code Optimization, 2015, 12, 1-23.	2.0	5
16	Dynamic front-end sharing in graphics processing units. , 2014, , .		3
17	HFA: A Hint Frequency-based approach to enhance the I/O performance of multi-level cache storage systems. , 2014, , .		5
18	Compiler assisted dynamic register file in GPGPU. , 2013, , .		20

#	Article	IF	Citations
19	AgileRegulator: A hybrid voltage regulator scheme redeeming dark silicon for power efficiency in a multicore architecture. , 2012, , .		40
20	ReVIVaL: A Variation-Tolerant Architecture Using Voltage Interpolation and Variable Latency. , 2008, , .		27
21	ReVIVaL. Computer Architecture News, 2008, 36, 191-202.	2.5	20
22	Architectural power models for sram and cam structures based on hybrid analytical/empirical techniques. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2007, , .	0.0	5
23	Process Variation Tolerant 3T1D-Based Cache Architectures. , 2007, , .		253
24	Process Variation Tolerant 3T1D-Based Cache Architectures. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2007, , .	0.0	1
25	Mitigating the Impact of Process Variations on Processor Register Files and Execution Units. Microarchitecture (MICRO), Proceedings of the Annual International Symposium on, 2006, , .	0.0	71
26	Microarchitecture Parameter Selection To Optimize System Performance Under Process Variation. IEEE/ACM International Conference on Computer-Aided Design, Digest of Technical Papers, 2006, , .	0.0	6