Xi Li

List of Publications by Year
in descending order

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71	642	687335	677123
papers	citations	13 h-index	22 g-index

71	71	71	504
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	MALOC: A Fully Pipelined FPGA Accelerator for Convolutional Neural Networks With All Layers Mapped on Chip. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 2601-2612.	2.7	82
2	Soft computing in big data intelligent transportation systems. Applied Soft Computing Journal, 2016, 38, 1099-1108.	7.2	64
3	Accelerating the Next Generation Long Read Mapping with the FPGA-Based System. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2014, 11, 840-852.	3.0	43
4	Service-Oriented Architecture on FPGA-Based MPSoC. IEEE Transactions on Parallel and Distributed Systems, 2017, 28, 2993-3006.	5.6	39
5	Heterogeneous Cloud Framework for Big Data Genome Sequencing. IEEE/ACM Transactions on Computational Biology and Bioinformatics, 2015, 12, 166-178.	3.0	33
6	Definitions of predictability for Cyber Physical Systems. Journal of Systems Architecture, 2016, 63, 48-60.	4.3	29
7	A Ubiquitous Machine Learning Accelerator With Automatic Parallelization on FPGA. IEEE Transactions on Parallel and Distributed Systems, 2020, 31, 2346-2359.	5.6	28
8	MP-Tomasulo. Transactions on Architecture and Code Optimization, 2013, 10, 1-26.	2.0	25
9	Architecture Support for Task Out-of-Order Execution in MPSoCs. IEEE Transactions on Computers, 2015, 64, 1296-1310.	3.4	23
10	SODA: Software Defined FPGA based Accelerators for Big Data. , 2015, , .		23
11	FreeRider: Non-Local Adaptive Network-on-Chip Routing with Packet-Carried Propagation of Congestion Information. IEEE Transactions on Parallel and Distributed Systems, 2015, 26, 2272-2285.	5.6	20
12	A star network approach in heterogeneous multiprocessors system on chip. Journal of Supercomputing, 2012, 62, 1404-1424.	3.6	18
13	Regarding Processors and Reconfigurable IP Cores as Services. , 2012, , .		18
14	Colored Petri Net model with automatic parallelization on real-time multicore architectures. Journal of Systems Architecture, 2014, 60, 293-304.	4.3	18
15	A High-Performance Accelerator for Large-Scale Convolutional Neural Networks. , 2017, , .		17
16	Hardware Implementation on FPGA for Task-Level Parallel Dataflow Execution Engine. IEEE Transactions on Parallel and Distributed Systems, 2016, 27, 2303-2315.	5.6	16
17	Implementation and Optimization of the Accelerator Based on FPGA Hardware for LSTM Network. , 2017, , .		12
18	WooKong: A Ubiquitous Accelerator for Recommendation Algorithms with Custom Instruction Sets on FPGA. IEEE Transactions on Computers, 2020, , 1-1.	3.4	11

#	Article	IF	Citations
19	Improving HW/SW Adaptability for Accelerating CNNs on FPGAs through A Dynamic/Static Co-Reconfiguration Approach. IEEE Transactions on Parallel and Distributed Systems, 2020, , 1-1.	5.6	11
20	Hardware acceleration for the banded Smith-Waterman algorithm with the cycled systolic array. , 2013, , .		9
21	Refactoring Network Functions Modules to Reduce Latencies and Improve Fault Tolerance in NFV. IEEE Journal on Selected Areas in Communications, 2018, 36, 2275-2287.	14.0	9
22	SCADIS: A Scalable Accelerator for Data-Intensive String Set Matching on FPGAs. , 2016, , .		8
23	SOLAR: Services-Oriented Learning Architectures. , 2016, , .		8
24	An FPGA-Based Accelerator for Neighborhood-Based Collaborative Filtering Recommendation Algorithms. , 2015, , .		7
25	An Intelligent Transportation System Using RFID Based Sensors. , 2013, , .		4
26	SOBA: A Services-Oriented Browser Architecture with Distributed URL-Filtering Mechanisms for Teenagers. , 2013, , .		4
27	PIE: A Pipeline Energy-Efficient Accelerator for Inference Process in Deep Neural Networks. , 2016, , .		4
28	A Power-Efficient Accelerator for Convolutional Neural Networks. , 2017, , .		4
29	A Time-Aware Programming Framework for Constructing Predictable Real-Time Systems. , 2017, , .		4
30	SmartClass: A Services-Oriented Approach for University Resource Scheduling. , 2013, , .		3
31	FairPlay: Services Migration with Lock-Free Mechanisms for Load Balancing in Cloud Architectures. , 2016, , .		3
32	Work-in-Progress: TTI: A Timing ISA for LET Model in Safety-Critical Systems. , 2017, , .		3
33	A Predictable Servant-Based Execution Model for Safety-Critical Systems. , 2017, , .		3
34	A FPGA-Based High Performance Acceleration Platform for the Next Generation Long Read Mapping. , 2013, , .		2
35	Static or Dynamic: Trade-Offs for Task Dependency Analysis for Heterogeneous MPSoC. , 2013, , .		2
36	SmartMal: A Service-Oriented Behavioral Malware Detection Framework for Mobile Devices. Scientific World Journal, The, 2014, 2014, 1-11.	2.1	2

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37	Towards Energy Optimization Based on Delay-Sensitive Traffic for WiFi Network. , 2014, , .		2
38	Amdahl's and Hill-Marty laws revisited for FPGA-based MPSoCs: from theory to practice. International Journal of High Performance Systems Architecture, 2014, 5, 115.	0.3	2
39	Codem: software/hardware codesign for embedded multicore systems supporting hardware services. International Journal of Electronics, 2015, 102, 32-47.	1.4	2
40	CRAIS: A Crossbar-Based Interconnection Scheme on FPGA for Big Data. Journal of Computer Science and Technology, 2015, 30, 84-96.	1.5	2
41	xFilter: A Temporal Locality Accelerator for Intrusion Detection System Services. , 2017, , .		2
42	UniCNN: A Pipelined Accelerator Towards Uniformed Computing for CNNs. International Journal of Parallel Programming, 2018, 46, 776-787.	1.5	2
43	CRAIS: A Crossbar Based Adaptive Interconnection Scheme. Lecture Notes in Computer Science, 2012, , 379-384.	1.3	2
44	UH-JLS: A Parallel Ultra-High Throughput JPEG-LS Encoding Architecture for Lossless Image Compression. , 2021, , .		2
45	Enabling Fast and Memory-Efficient Acceleration for Pattern Matching Workloads: The Lightweight Automata Processing Engine. IEEE Transactions on Computers, 2023, 72, 1011-1025.	3.4	2
46	Parallel dataflow execution for sequential programs on reconfigurable hybrid MPSoCs. , 2012, , .		1
47	A Semantics-based Translation Method for Automated Verification of SystemC TLM Designs. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 685-695.	1.2	1
48	FPGA implementation of a scheduler supporting parallel dataflow execution. , 2013, , .		1
49	Detecting Associations in Large Dataset on MapReduce. , 2013, , .		1
50	Kernel-User Space Separation in DRAM Memory. , 2014, , .		1
51	Application-aware group scheduler for Android. , 2014, , .		1
52	PUMA: From Simultaneous to Parallel for Shared Memory System in Multi-core. Journal of Signal Processing Systems, 2016, 84, 139-150.	2.1	1
53	Hot spots profiling and dataflow analysis in custom dataflow computing SoftProcessors. Journal of Systems and Software, 2017, 125, 427-438.	4.5	1
54	Clockwerk: A Predictable and Efficient Extension of Logical Execution Time Model. , 2017, , .		1

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55	Exploiting Aperiodic Server to Improve Aperiodic Responsiveness for LET-Based Real-Time Systems. , 2017, , .		1
56	Tickwerk: Design of a LET-Based SoC for Temporal Programming. , 2017, , .		1
57	GenServ: Genome Sequencing Services on Scalable Energy Efficient Accelerators. , 2017, , .		1
58	3D Waveform Oscilloscope Implemented on Coupled FPGA-GPU Embedded System. , 2018, , .		1
59	Supporting Predictable Servant-Based Execution Model on Multicore Platforms. , 2018, , .		1
60	WiderFrame: An Automatic Customization Framework for Building CNN Accelerators on FPGAs: Work-in-Progress. , 2020, , .		1
61	Group Scheduling for Improving Both CPU and Memory Power Efficiency Simultaneously. , 2013, , .		0
62	Trade-offs between the sensitivity and the speed of the FPGA-based sequence aligner. , 2014, , .		0
63	PUMA: Pseudo unified memory architecture for single-ISA heterogeneous multi-core systems. , 2014, , .		0
64	Multi-objective aware design flow for coarse-grained systems on chip. , 2014, , .		0
65	Memory power optimization on different memory address mapping schemas. , 2014, , .		0
66	A case study of parallel JPEG encoding on an FPGA. Journal of Parallel and Distributed Computing, 2015, 78, 1-5.	4.1	0
67	Rethinking Energy-Efficiency of Heterogeneous Computing for CNN-Based Mobile Applications. , 2017, , .		0
68	Building a Game Benchmark for Cooperative CPU-GPU with Pseudo User-Interaction. , 2017, , .		0
69	Instruction Extension and Generation for Adaptive Processors. Lecture Notes in Computer Science, 2014, , 306-311.	1.3	0
70	Effective and Efficient Design Space Exploration for Heterogeneous Microprocessor Systems-on-Chip. , 2015, , 3-26.		0
71	DCW. ACM Transactions on Design Automation of Electronic Systems, 2019, 24, 1-35.	2.6	0