Hyungcheol Shin

List of Publications by Year in Descending Order

142 papers	1,490 citations	22 h-index	32 g-index
184 ext. papers	1,737 ext. citations	2.5 avg, IF	4.47 L-index

#	Paper	IF	Citations
142	Investigation and Modeling of Z-Interference in Poly-Si Channel-Based 3-D NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2022**, 69, 543-548	2.9	1
141	Analysis and Compact Modeling of Fast Detrapping From Bandgap-Engineered Tunneling Oxide in 3-D NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2021**, 68, 3339-3345	2.9	1
140	Investigation and Compact Modeling of Hot-Carrier Injection for Read Disturbance in 3-D NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2020**, 67, 2778-2784	2.9	5
139	A Compact Model for ISPP of 3-D Charge-Trap NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2020**, 67, 3095-3101	2.9	5
138	Separation of Lateral Migration Components by Hole During the Short-Term Retention Operation in 3-D NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2020**, 67, 2645-2647	2.9	3
137	Extraction of Mobility in 3-D NAND Flash Memory with Poly-Si Based Macaroni Structure **2020**,		3
136	Variability-Aware Machine Learning Strategy for 3-D NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2020**, 67, 1575-1580	2.9	8
135	A Simple and Accurate Modeling Method of Channel Thermal Noise Using BSIM4 Noise Models. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, **2020**, 39, 4351-4358	2.5	1
134	Self-Heating and Electrothermal Properties of Advanced Sub-5-nm Node Nanoplate FET. *IEEE Electron Device Letters*, **2020**, 41, 977-980	4.4	8
133	Machine learning model for predicting threshold voltage by taper angle variation and word line position in 3D NAND flash memory. *IEICE Electronics Express*, **2020**, 17, 20200345-20200345	0.5	1
132	Comparative Analysis of Hot Carrier Degradation (HCD) in 10-nm Node nMOS/pMOS FinFET Devices. *IEEE Transactions on Electron Devices*, **2020**, 67, 5396-5402	2.9	3
131	Methodology to Predict Random Telegraph Noise Induced Threshold Voltage Shift Using Machine Learning **2020**,		1
130	Investigation and SPICE Compact Model of Spacer Region for Static Characteristics of 3-D NAND Flash Memories. *IEEE Transactions on Electron Devices*, **2020**, 67, 4158-4165	2.9	3
129	Cell Pattern Dependency of Charge Failure Mechanisms During Short-Term Retention in 3-D NAND Flash Memories. *IEEE Electron Device Letters*, **2020**, 41, 1645-1648	4.4	3
128	Strain Engineering for 3.5-nm Node in Stacked-Nanoplate FET. *IEEE Transactions on Electron Devices* , **2019**, 66, 2898-2903	2.9	8
127	Modeling of Lateral Migration Mechanism During the Retention Operation in 3D NAND Flash Memories **2019**,		6
126	Investigation of Gate Sidewall Spacer Optimization From OFF-State Leakage Current Perspective in 3-nm Node Device. *IEEE Transactions on Electron Devices*, **2019**, 66, 2532-2537	2.9	9

125	BSIM-CMG Modeling for 3D NAND Cell with Macaroni Channel **2019**,		2
124	Compact Model Strategy of Metal-Gate Work-Function Variation for Ultrascaled FinFET and Vertical GAA FETs. *IEEE Transactions on Electron Devices*, **2019**, 66, 1613-1616	2.9	14
123	Variability-Aware Simulation Strategy for Gate-All-Around Vertical Field Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6715-6721	1.3	
122	Modeling of Nanoplate Parasitic Extension Resistance and its Associated Dependency on Spacer Materials. *IEEE Transactions on Electron Devices*, **2019**, 66, 2527-2531	2.9	1
121	Effect of Various Geometry Parameters on the Performance of Nanoplate Field Effect Transistor with Negative Capacitance. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6736-6740	1.3	
120	Device Optimization of Nano-Plate Transistors for 3.5 nm Technology Node. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6771-6775	1.3	
119	Fringe Capacitance Modeling in NanoPlate MOSFET Using Conformal Mapping. *IEEE Transactions on Electron Devices*, **2019**, 66, 2446-2449	2.9	3
118	Analysis of Variation and Ferroelectric Layer Thickness on Negative Capacitance Nanowire Field-Effect Transistor. *Journal of Nanoscience and Nanotechnology*, **2019**, 19, 6710-6714	1.3	1
117	Modeling of Lateral Migration Mechanism of Holes in 3D NAND Flash Memory Charge Trap Layer during Retention Operation **2019**,		2
116	Thermal-Aware Shallow Trench Isolation Design Optimization for Minimizing ${I}_{OFF}$ in Various Sub-10-nm 3-D Transistors. *IEEE Transactions on Electron Devices*, **2019**, 66, 647-654	2.9	8
115	Prediction of Alpha Particle Effect on 5-nm Vertical Field-Effect Transistors. *IEEE Transactions on Electron Devices*, **2019**, 66, 806-809	2.9	2
114	Device Investigation of Nanoplate Transistor With Spacer Materials. *IEEE Transactions on Electron Devices*, **2019**, 66, 766-770	2.9	9
113	Analysis of Electrothermal Characteristics of GAA Vertical Nanoplate-Shaped FETs. *IEEE Transactions on Electron Devices*, **2018**, 65, 3061-3064	2.9	13
112	Analysis on Self-Heating Effects in Three-Stacked Nanoplate FET. *IEEE Transactions on Electron Devices*, **2018**, 65, 4520-4526	2.9	14
111	Analysis and Comparison of Interface Trap for Single and 3D Stacked Nanowire FET. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7121-7125	1.3	1
110	Analysis on DC and AC Characteristics of Self Heating Effect in Nanowire. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 3056-3059	1.3	2
109	Investigation of Work Function Variation Induced by Metal Gate and Process Variation Effect in 3D Stacked Nanowire FET Devices. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7115-7120	1.3	
108	Comparison for Performance and Reliability Between Nanowire FET and FinFET versus Technology Node. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7227-7230	1.3	0

107	Line Edge Roughness and Process Variation Effect of Three Stacked Gate-All-Around Silicon MOSFET Devices. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 7130-7133	1.3	0
106	Various Extraction Methods for Parasitic Capacitances in Nanowire FET. *Journal of Nanoscience and Nanotechnology*, **2017**, 17, 3051-3055	1.3	
105	Accurate Lifetime Estimation of Sub-20-nm NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2016**, 63, 659-667	2.9	19
104	Separation of Corner Component in TAT Mechanism in Retention Characteristics of Sub 20-nm NAND Flash Memory. *IEEE Electron Device Letters*, **2014**, 35, 51-53	4.4	12
103	Probability Level Dependence of Failure Mechanisms in Sub-20 nm NAND Flash Memory. *IEEE Electron Device Letters*, **2014**, 35, 348-350	4.4	6
102	Is quantum capacitance in graphene a potential hurdle for device scaling?. *Nano Research*, **2014**, 7, 453-461	7.9	8
101	Analysis of failure mechanisms in erased state of sub 20-nm NAND Flash memory **2014**,		10
100	Analysis of Failure Mechanisms and Extraction of Activation Energies (E_{a}) in 21-nm nand Flash Cells. *IEEE Electron Device Letters*, **2013**, 34, 48-50	4.4	23
99	Correction to Generation Dependence of Retention Characteristics in Extremely Scaled NAND Flash Memory[Sep 13 1139-1141]. *IEEE Electron Device Letters*, **2013**, 34, 1345-1345	4.4	
98	Activation Energies (E_{a}) of Failure Mechanisms in Advanced NAND Flash Cells for Different Generations and Cycling. *IEEE Transactions on Electron Devices*, **2013**, 60, 1099-1107	2.9	27
97	Capture Cross Section of Traps Causing Random Telegraph Noise in Gate-Induced Drain Leakage Current. *IEEE Transactions on Electron Devices*, **2013**, 60, 1268-1271	2.9	6
96	Generation Dependence of Retention Characteristics in Extremely Scaled NAND Flash Memory. *IEEE Electron Device Letters*, **2013**, 34, 1139-1141	4.4	17
95	L-Shaped Tunneling Field-Effect Transistors for Complementary Logic Applications. *IEICE Transactions on Electronics*, **2013**, E96.C, 634-638	0.4	1
94	. *IEEE Transactions on Electron Devices*, **2012**, 59, 35-45	2.9	50
93	Extraction of Location and Energy Level of the Trap Causing Random Telegraph Noise at Reverse-Biased Region in GaN-Based Light-Emitting Diodes. *IEEE Transactions on Electron Devices*, **2012**, 59, 3495-3502	2.9	6
92	63.4: Extraction of the Location and the Energy Level of the Trap using Random Telegraph Noise in GaN-based Light-Emitting Diode. *Digest of Technical Papers SID International Symposium*, **2012**, 43, 865-868	0.5	1
91	Poly-silicon quantum-dot single-electron transistors. *Journal of the Korean Physical Society*, **2012**, 60, 108-112	0.6	1
90	Compact modeling of extremely scaled graphene FETs. *Journal of the Korean Physical Society*, **2012**, 61, 1797-1801	0.6	3

89	The Compact Modeling of Channel Potential in Sub-30-nm NAND Flash Cell String. *IEEE Electron Device Letters*, **2012**, 33, 321-323	4.4	19
88	An Accurate Compact Model Considering Direct-Channel Interference of Adjacent Cells in Sub-30-nm nand Flash Technologies. *IEEE Electron Device Letters*, **2012**, 33, 1114-1116	4.4	19
87	Characterization of Border Trap Density With the Multifrequency Charge Pumping Technique in Dual-Layer Gate Oxide. *IEEE Transactions on Electron Devices*, **2011**, 58, 2752-2758	2.9	7
86	DIBL-Induced Program Disturb Characteristics in 32-nm NAND Flash Memory Array. *IEEE Transactions on Electron Devices*, **2011**, 58, 3626-3629	2.9	8
85	Single-Crystalline Si STacked ARray (STAR) NAND Flash Memory. *IEEE Transactions on Electron Devices*, **2011**, 58, 1006-1014	2.9	21
84	Trench-type deep N-well dual guard ring for the suppression of substrate noise coupling. *International Journal of RF and Microwave Computer-Aided Engineering*, **2011**, 21, 36-44	1.5	2
83	Experimental Investigation of Quasi-Ballistic Carrier Transport Characteristics in 10-nm Scale MOSFETs. *IEEE Nanotechnology Magazine*, **2011**, 10, 975-979	2.6	2
82	A Simple Model for Capture and Emission Time Constants of Random Telegraph Signal Noise. *IEEE Nanotechnology Magazine*, **2011**, 10, 1352-1356	2.6	5
81	Non-ideal characteristic analysis of GaN-based light-emitting diode using current-voltage (I□V) and low-frequency noise experiment **2011**,		1
80	Investigation of Gate Etch Damage at Metal/High-k Gate Dielectric Stack Through Random Telegraph Noise in Gate Edge Direct Tunneling Current. *IEEE Electron Device Letters*, **2011**, 32, 569-571	4.4	13
79	Study of slow oxide trap creating random telegraph noise within a gate edge overlap region in inversion mode. *Applied Physics Letters*, **2011**, 99, 232904	3.4	1
78	Accurate extraction of □/I due to random telegraph noise in gate edge current of high-k n-type metal-oxide-semiconductor field-effect transistors under accumulation mode. *Applied Physics Letters*, **2011**, 98, 023505	3.4	3
77	Improving Read Disturb Characteristics by Using Double Common Source Line and Dummy Switch Architecture in Multi Level Cell NAND Flash Memory with Low Power Consumption. *Japanese Journal of Applied Physics*, **2011**, 50, 04DD03	1.4	3
76	Effects of aluminum layer and oxidation on TiO2 based bipolar resistive random access memory (RRAM) **2010**,		1
75	Characterization of random telegraph noise in gate induced drain leakage current of n- and p-type metal-oxide-semiconductor field-effect transistors. *Applied Physics Letters*, **2010**, 96, 043502	3.4	10
74	Observation of three-level random telegraph noise in GIDL current of Saddle-Fin type DRAM cell transistor **2010**,		1
73	Device and Circuit Codesign Strategy for Application to Low-Noise Amplifier Based on Silicon Nanowire Metal□Oxide□Semiconductor Field Effect Transistors. *Japanese Journal of Applied Physics*, **2010**, 49, 04DN03	1.4	1
72	Low noise capacitive sensor for multi-touch mobile handset's applications **2010**,		1

71	A study on the carrier injection mechanism of the bottom-contact pentacene thin film transistor. *Applied Physics Letters*, **2010**, 96, 103305	3.4	23
70	A Vertical 4-Bit SONOS Flash Memory and a Unique 3-D Vertical nor Array Structure. *IEEE Nanotechnology Magazine*, **2010**, 9, 70-77	2.6	9
69	Electrical instabilities and low-frequency noise in InGaZnO thin film transistors **2010**,		2
68	Characterization of oxide traps by RTN measurement in MOSFETs and memory devices **2010**,		3
67	A comparative study of the program efficiency of gate all around SONOS and TANOS flash memory **2010**,		1
66	RF performance of pre-patterned locally-embedded-back-gate graphene device **2010**,		10
65	Investigation of Random Telegraph Noise in Gate-Induced Drain Leakage and Gate Edge Direct Tunneling Currents of High-k MOSFETs. *IEEE Transactions on Electron Devices*, **2010**, 57, 913-918	2.9	19
64	Simulation Study on Dependence of Channel Potential Self-Boosting on Device Scale and Doping Concentration in 2-D and 3-D NAND-Type Flash Memory Devices. *IEICE Transactions on Electronics*, **2010**, E93-C, 596-601	0.4	
63	Simulation study for suppressing corner effect in a saddle MOSFET for Sub-50 nm high density high performance DRAM cell transistor **2009**,		1
62	RTS-like fluctuation in Gate Induced Drain Leakage current of Saddle-Fin type DRAM cell transistor **2009**,		12
61	Accurate Extraction of Excess Channel Thermal Noise Coefficient in Berkeley Short-Channel Insulated Gate Field-Effect Transistor Model 4. *Japanese Journal of Applied Physics*, **2009**, 48, 04C037	1.4	
60	Modeling and Parameter Extraction for the Series Resistance in Thin-Film Transistors. *IEEE Transactions on Electron Devices*, **2009**, 56, 431-440	2.9	24
59	Independent Double-Gate Fin SONOS Flash Memory Fabricated With Sidewall Spacer Patterning. *IEEE Transactions on Electron Devices*, **2009**, 56, 1721-1728	2.9	13
58	. *IEEE Transactions on Electron Devices*, **2009**, 56, 2489-2495	2.9	13
57	Low power size-efficient CMOS UWB low-noise amplifier design. *Microwave and Optical Technology Letters*, **2009**, 51, 494-496	1.2	
56	0.7 V supply highly linear subthreshold low-noise amplifier design for 2.4 GHz wireless sensor network applications. *Microwave and Optical Technology Letters*, **2009**, 51, 1316-1320	1.2	3
55	Size efficient low-noise amplifier for 2.4 GHz ISM-band transceiver. *Microwave and Optical Technology Letters*, **2009**, 51, 2304-2308	1.2	
54	Deembedding Accuracy for Device Scale and Interconnection Line Parasitics. *IEEE Microwave and Wireless Components Letters*, **2009**, 19, 713-715	2.6	2

53	Characterization of oxide traps leading to RTN in high-k and metal gate MOSFETs **2009**,		6
52	Application of the Compact Channel Thermal Noise Model of Short Channel MOSFETs to CMOS RFIC Design. *IEICE Transactions on Electronics*, **2009**, E92-C, 627-634	0.4	1
51	3-Dimensional Terraced NAND (3D TNAND) Flash Memory-Stacked Version of Folded NAND Array. *IEICE Transactions on Electronics*, **2009**, E92-C, 653-658	0.4	1
50	Simulation of Retention Characteristics in Double-Gate Structure Multi-Bit SONOS Flash Memory. *IEICE Transactions on Electronics*, **2009**, E92-C, 659-663	0.4	0
49	A Simple Figure of Merit of RF MOSFET for Low-Noise Amplifier Design. *IEEE Electron Device Letters* , **2008**, 29, 1380-1382	4.4	27
48	A capacitor-less 1T-DRAM cell with vertical surrounding gates using gate-induced drain-leakage (GIDL) current **2008**,		3
47	On the Characteristics and Spatial Dependence of Channel Thermal Noise in Nanoscale Metal□Oxide□Semiconductor Field Effect Transistors. *Japanese Journal of Applied Physics*, **2008**, 47, 2636-2640	1.4	3
46	Optimization of cascode configuration in CMOS low-noise amplifier. *Microwave and Optical Technology Letters*, **2008**, 50, 646-649	1.2	13
45	Small size low noise amplifier with suppressed noise from gate resistance. *Microwave and Optical Technology Letters*, **2008**, 50, 2300-2304	1.2	
44	A low power low noise amplifier with subthreshold operation in 130 nm CMOS technology. *Microwave and Optical Technology Letters*, **2008**, 50, 2762-2764	1.2	1
43	Admittance Measurements on OFET Channel and Its Modeling With R□C$ Network. *IEEE Electron Device Letters*, **2007**, 28, 204-206	4.4	23
42	Extraction of pi-Type Substrate Resistance Based on Three-Port Measurement and the Model Verification up to 110 GHz. *IEEE Electron Device Letters*, **2007**, 28, 425-427	4.4	7
41	A New Noise Parameter Model of Short-Channel MOSFETs. *Radio Frequency Integrated Circuits (RFIC) Symposium, IEEE*, **2007**,		8
40	A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell). *IEEE Nanotechnology Magazine*, **2007**, 6, 352-357	2.6	31
39	An analytical channel thermal noise model for deep-submicron MOSFETs with short channel effects. *Solid-State Electronics*, **2007**, 51, 1034-1038	1.7	22
38	Separate Extraction of Gate Resistance Components in RF MOSFETs. *IEEE Transactions on Electron Devices*, **2007**, 54, 1459-1463	2.9	21
37	A novel gated transmission line method for organic thin film transistors **2007**,		1
36	Fin width variation effects on program disturbance characteristics in a NAND type bulk fin SONOS flash memory **2007**,		1

35	2.4 GHz ISM-Band Receiver Design in a 0.18 $mu{hbox{m}}$ Mixed Signal CMOS Process. *IEEE Microwave and Wireless Components Letters*, **2007**, 17, 736-738	2.6	5
34	Improving the Endurance Characteristics Through Boron Implant at Active Edge in 1 G NAND Flash **2007**,		3
33	Active and Passive RF Device Compact Modeling in CMOS Technoloies **2006**,		2
32	Non-quasi-static small-signal modeling and analytical parameter extraction of SOI FinFETs. *IEEE Nanotechnology Magazine*, **2006**, 5, 205-210	2.6	63
31	Low hysteresis pentacene thin-film transistors using SiO2/cross-linked poly(vinyl alcohol) gate dielectric. *Applied Physics Letters*, **2006**, 89, 263507	3.4	31
30	Design and optimization of two-bit double-gate nonvolatile memory cell for highly reliable operation. *IEEE Nanotechnology Magazine*, **2006**, 5, 180-185	2.6	7
29	Complete high-frequency thermal noise modeling of short-channel MOSFETs and design of 5.2-GHz low noise amplifier. *IEEE Journal of Solid-State Circuits*, **2005**, 40, 726-735	5.5	49
28	Extraction and modeling of gate electrode resistance in rf MOSFETs **2005**,		1
27	P-18: Performance Improvement of Scaled-down Top-contact OTFTs by Two-Step-Deposition of Pentacene. *Digest of Technical Papers SID International Symposium*, **2005**, 36, 292	0.5	1
26	A simple parameter extraction method of spiral on-chip inductors. *IEEE Transactions on Electron Devices*, **2005**, 52, 1976-1981	2.9	31
25	Performance improvement of scaled-down top-contact OTFTs by two-step-deposition of pentacene. *IEEE Electron Device Letters*, **2005**, 26, 903-905	4.4	10
24	Analytical drain thermal noise current model valid for deep submicron MOSFETs. *IEEE Transactions on Electron Devices*, **2004**, 51, 261-269	2.9	75
23	The effects of deuterium annealing on the reduction of dark currents in the CMOS APS. *IEEE Transactions on Electron Devices*, **2004**, 51, 1346-1349	2.9	14
22	Drain current thermal noise modeling for deep submicron n- and p-channel MOSFETs. *Solid-State Electronics*, **2004**, 48, 2255-2262	1.7	7
21	A simple wide-band on-chip inductor model for silicon-based RF ICs. *IEEE Transactions on Microwave Theory and Techniques*, **2003**, 51, 2023-2028	4.1	54
20	An RF model of the accumulation-mode MOS varactor valid in both accumulation and depletion regions. *IEEE Transactions on Electron Devices*, **2003**, 50, 1997-1999	2.9	27
19	A simple four-terminal small-signal model of RF MOSFETs and its parameter extraction. *Microelectronics Reliability*, **2003**, 43, 601-609	1.2	20
18	Gate bias dependence of the substrate signal coupling effect in RF MOSFETs. *IEEE Electron Device Letters*, **2003**, 24, 183-185	4.4	9

17	Thermal noise modeling for short-channel MOSFETs **2003**,		1
16	A -119.2 dBc/Hz at 1 MHz, 1.5 mW, fully integrated, 2.5-GHz, CMOS VCO using helical inductors. *IEEE Microwave and Wireless Components Letters*, **2003**, 13, 457-459	2.6	22
15	Accurate four-terminal RF MOSFET model accounting for the short-channel effect in the source-to-drain capacitance **2003**,		1
14	13 GHz 4.67 dB NF CMOS low-noise amplifier. *Electronics Letters*, **2003**, 39, 1056	1.1	19
13	A simple and analytical parameter-extraction method of a microwave MOSFET. *IEEE Transactions on Microwave Theory and Techniques*, **2002**, 50, 1503-1509	4.1	87
12	DC and AC characteristics of sub-50-nm MOSFETs with source/drain-to-gate nonoverlapped structure. *IEEE Nanotechnology Magazine*, **2002**, 1, 219-225	2.6	23
11	A simple and accurate method for extracting substrate resistance of RF MOSFETs. *IEEE Electron Device Letters*, **2002**, 23, 434-436	4.4	34
10	MOSFET MODELING AND PARAMETER EXTRACTION FOR RF IC'S. *Selected Topics in Electornics and Systems*, **2002**, 67-120	0	9
9	Characteristics of p-channel Si nano-crystal memory. *IEEE Transactions on Electron Devices*, **2001**, 48, 874-879	2.9	30
8	50 nm MOSFET with electrically induced source/drain (S/D) extensions. *IEEE Transactions on Electron Devices*, **2001**, 48, 2058-2064	2.9	14
7	Programming characteristics of p-channel Si nano-crystal memory. *IEEE Electron Device Letters*, **2000**, 21, 313-315	4.4	12
6	Room temperature single electron effects in a Si nano-crystal memory. *IEEE Electron Device Letters*, **1999**, 20, 630-631	4.4	49
5	A simple technique to measure generation lifetime in partially depleted SOI MOSFETs. *IEEE Transactions on Electron Devices*, **1998**, 45, 2378-2380	2.9	12
4	Photocurrent effect on the zero-Bias dynamic resistance of HgCdTe photodiode. *Journal of Electronic Materials*, **1997**, 26, 662-666	1.9	2
3	A direct method to extract the substrate resistance components of RF MOSFETs valid up to 50 GHz		5
2	A scalable model for the substrate resistance in multi-finger RF MOSFETs		3
1	Effects of S/D non-overlap and high-/spl kappa/ dielectrics on nano CMOS design		2