Isuru Nawinne

List of Publications by Year
in descending order

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6 papers	9 citations	3311381 1 h-index	2917675 2 g-index

6 all docs	6 docs citations	6 times ranked	13 citing authors

#	Article	IF	Citations
1	Latency-constrained binding of data flow graphs to energy conscious GALS-based MPSoCs. , 2013, , .		2
2	Hardware-based fast exploration of cache hierarchies in application specific MPSoCs. , 2014, , .		2
3	Exploring Multilevel Cache Hierarchies in Application Specific MPSoCs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2015, 34, 1991-2003.	2.7	2
4	A survey on exact cache design space exploration methodologies for application specific SoC memory hierarchies. , 2013, , .		1
5	Hardware-based fast exploration of cache hierarchies in application specific MPSoCs. , 2014, , .		1
6	Switchable cache: utilising dark silicon for application specific cache optimisations. IET Computers and Digital Techniques, 2016, 10, 157-164.	1.2	1