Haruo Kobayashi, å°æ—æ˜¥å¤«

List of Publications by Year
in descending order

90 papers	798 citations	1040056 9 h-index	752698 20 g-index
90 all docs	90 docs citations	90 times ranked	420 citing authors

#	Article	IF	Citations
1	CMOS Circuits to Measure Timing Jitter Using a Self-Referenced Clock and a Cascaded Time Difference Amplifier With Duty-Cycle Compensation. IEEE Journal of Solid-State Circuits, 2012, 47, 2701-2710.	5.4	113
2	Graphene field-effect transistor biosensor for detection of biotin with ultrahigh sensitivity and specificity. Biosensors and Bioelectronics, 2020, 165, 112363.	10.1	70
3	SAR ADC algorithm with redundancy. , 2008, , .		45
4	SAR ADC Algorithm with Redundancy and Digital Error Correction. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 415-423.	0.3	39
5	Low-distortion signal generation for ADC testing. , 2014, , .		33
6	Sampling clock jitter effects in digital-to-analog converters. Measurement: Journal of the International Measurement Confederation, 2002, 31, 187-199.	5.0	27
7	Stochastic TDC architecture with self-calibration. , 2010, , .		23
8	Low-Distortion Sinewave Generation Method Using Arbitrary Waveform Generator. Journal of Electronic Testing: Theory and Applications (JETTA), 2012, 28, 641-651.	1.2	22
9	Total Harmonic Distortion Measurement System of Electronic Devices up to 100 MHz With Remarkable Sensitivity. IEEE Transactions on Instrumentation and Measurement, 2007, 56, 2360-2368.	4.7	18
10	I-Q signal generation techniques for communication IC testing and ATE systems. , 2016, , .		17
11	Successive approximation time-to-digital converter with vernier-level resolution. , 2016, , .		16
12	Analysis of Coupled Inductors for Low-Ripple Fast-Response Buck Converter. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 451-455.	0.3	16
13	ADC linearity test signal generation algorithm. , 2010, , .		15
14	High-frequency low-distortion signal generation algorithm with arbitrary waveform generator. , 2015, , .		15
15	Multi-bit Sigma-Delta TDC Architecture with Improved Linearity. Journal of Electronic Testing: Theory and Applications (JETTA), 2013, 29, 879-892.	1.2	14
16	Low-Distortion Single-Tone and Two-Tone Sinewave Generation Algorithms Using an Arbitrary Waveform Generator. , 2011, , .		13
17	Avidinâ€“Biotin Technology in Gold Nanoparticle-Decorated Graphene Field Effect Transistors for Detection of Biotinylated Macromolecules with Ultrahigh Sensitivity and Specificity. ACS Omega, 2020, 5, 30037-30046.	3.5	13
18	Two-Tone Signal Generation for Communication Application ADC Testing. , 2012, , .		12

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19	Phase noise measurement techniques using delta-sigma TDC. , 2014, , .		11
20	Experimental verification of timing measurement circuit with self-calibration. , 2014, , .		11
21	Using distortion shaping technique to equalize ADC THD performance between ATEs. , 2016, , .		10
22	Two-Tone Signal Generation for ADC Testing. IEICE Transactions on Electronics, 2013, E96.C, 850-858.	0.6	10
23	Analog/Mixed-Signal Circuit Testing Technologies in IoT Era. , 2020, , .		10
24	Finite Aperture Time and Sampling Jitter Effects in Wideband Data Acquisition Systems. , 2000, , .		9
25	SAR ADC Architecture with Digital Error Correction. IEEJ Transactions on Electrical and Electronic Engineering, 2010, 5, 651-659.	1.4	9
26	A Small Chip Area Stochastic Calibration for TDC Using Ring Oscillator. Journal of Electronic Testing: Theory and Applications (JETTA), 2014, 30, 653-663.	1.2	9
27	High-frequency low-distortion one-tone and two-tone signal generation using arbitrary waveform generator. , 2016, , .		9
28	High-resolution DPWM generator for digitally controlled DC-DC converters. , 2008, , .		8
29	Analog/mixed-signal circuit design in nano CMOS era. IEICE Electronics Express, 2014, 11, 20142001-20142001.	0.8	8
30	An on-chip timing jitter measurement circuit using a self-referenced clock and a cascaded time difference amplifier with duty-cycle compensation. , 2011, , .		7
31	A gray code based time-to-digital converter architecture and its FPGA implementation. , 2015, , .		7
32	Timing measurement BOST architecture with full digital circuit and self-calibration using characteristics variation positively for fine time resolution. , 2016, , .		7
33	Technique to Improve the Performance of Time-Interleaved A-D Converters with Mismatches of Non-linearity. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 374-380.	0.3	7
34	Single inductor dual output DC-DC converter design with exclusive control. , 2012, , .		6
35	A New Procedure for Measuring High-Accuracy Probability Density Functions. , 2012, , .		6
36	A CMOS PWM Transceiver Using Self-Referenced Edge Detection. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, 23, 1145-1149.	3.1	6

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37	Multitone curve-fitting algorithms for communication application ADC testing. Electronics and Communications in Japan, 2003, 86, 1-11.	0.2	5
38	Redundant SAR ADC Algorithm Based on Fibonacci Sequence. Key Engineering Materials, 2016, 698, 118-126.	0.4	5
39	Analysis and Design of Inverter-Type Gm-C Bandpass Filter. IEEJ Transactions on Electronics, Information and Systems, 2009, 129, 1483-1489.	0.2	5
40	Design for Testability That Reduces Linearity Testing Time of SAR ADCs. IEICE Transactions on Electronics, 2011, E94-C, 1061-1064.	0.6	5
41	EMI Reduction by Spread-Spectrum Clocking in Digitally-Controlled DC-DC Converters. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 1004-1011.	0.3	5
42	ADC standard and testing in Japanese industry. Computer Standards and Interfaces, 2001, 23, 57-64.	5.4	4
43	A New Control Method for Switched Buck-Boost DC-DC Converters with Delta-Sigma Modulation for Mobile Equipment. , 2006, , .		4
44	ΔΣAD modulator for low power application. , 2008, , .		4
45	Low-IMD Two-Tone Signal Generation for ADC Testing. , 2012, , .		4
46	Multi-bit Sigma-Delta TDC Architecture for Digital Signal Timing Measurement. , 2012, , .		4
47	Delta-Sigma Digital-to-Time Converter for Band-Select Spread Spectrum Clock. Key Engineering Materials, 2015, 643, 79-91.	0.4	4
48	Using Distortion Shaping Technique to Equalize ADC THD Performance Between ATEs. Journal of Electronic Testing: Theory and Applications (JETTA), 2017, 33, 295-303.	1.2	4
49	A Distortion Shaping Technique to Equalize Intermodulation Distortion Performance of Interpolating Arbitrary Waveform Generators in Automated Test Equipment. Journal of Electronic Testing: Theory and Applications (JETTA), 2018, 34, 215-232.	1.2	4
50	Low-Distortion One-Tone and Two-Tone Signal Generation Using AWG Over Full Nyquist Region. , 2018, , .		4
51	Performance Improvement of Delta-Sigma ADC/DAC/TDC Using Digital Technique. , 2018, , .		4
52	Analog / Mixed-Signal / RF Circuits for Complex Signal Processing. , 2019, , .		4
53	A Feed-Forward Time Amplifier Using a Phase Detector and Variable Delay Lines. IEICE Transactions on Electronics, 2013, E96.C, 920-922.	0.6	4
54	Revisit to Histogram Method for ADC Linearity Test: Examination of Input Signal and Ratio of Input and Sampling Frequencies. Journal of Electronic Testing: Theory and Applications (JETTA), 2022, 38, 21-38.	1.2	4

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55	Low-voltage rail-to-rail CMOS operational amplifier design. Electronics and Communications in Japan, 2006, 89, 1-7.	0.2	3
56	Second-order ΔΣAD modulator with novel feedforward architecture. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	3
57	Complex bandpass Î£Î”AD modulator with noise-coupled architecture. , 2008, , .		3
58	Analysis of coupled inductors for low-ripple fast-response buck converter. , 2008, , .		3
59	Production Test Considerations for Mixed-signal IC with Background Calibration. IEEJ Transactions on Electrical and Electronic Engineering, 2010, 5, 627-631.	1.4	3
60	Design of Fourth-Order Continuous-Time Bandpass Î”Î£AD Modulator for RF Sampling. IEEJ Transactions on Electrical and Electronic Engineering, 2010, 5, 639-645.	1.4	3
61	Digitally-Assisted Compensation Technique for Timing Skew in ATE Systems. , 2011, , .		3
62	Digitally-controlled Gm-C bandpass filter. , 2012, , .		3
63	Frequency Estimation Sampling Circuit Using Analog Hilbert Filter and Residue Number System. , 2019, , .		3
64	Input Signal and Sampling Frequencies Requirements for Efficient ADC Testing with Histogram Method. , 2021, , .		3
65	Fibonacci sequence weighted SAR ADC as golden section search. , 2017, , .		2
66	RC Polyphase Filter as Complex Analog Hilbert Filter. Applied Mechanics and Materials, 0, 888, 29-36.	0.2	2
67	Design and theoretical analysis of a clock jitter reduction circuit using gated phase blending between self-delayed clock edges. IEICE Electronics Express, 2019, 16, 20190218-20190218.	0.8	2
68	High-Frequency Low-Distortion One-Tone and Two-Tone Signal Generation Using Arbitrary Waveform Generator. Applied Mechanics and Materials, 0, 888, 52-58.	0.2	2
69	Cross-Noise-Coupled Architecture of Complex Bandpass .DELTA..SIGMA.AD Modulator. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2009, E92-A, 998-1003.	0.3	2
70	Noise-Coupled .DELTA..SIGMA.AD Modulator with Shared OP-Amp. IEEJ Transactions on Electronics, Information and Systems, 2009, 129, 2167-2173.	0.2	2
71	A Quasi-Coherent Sampling Method for Wideband Data Acquisition. , 2000, , .		1
72	A low-offset cascaded time amplifier with reconfigurable inter-stage connection. IEICE Electronics Express, 2014, 11, 20140203-20140203.	0.8	1

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73	Phase Noise Measurement and Testing with Delta-Sigma TDC. Key Engineering Materials, 2015, 643, 149-155.	0.4	1
74	Unified Methodology of Analog/Mixed-Signal IC Design Based on Number Theory. , 2018, , .		1
75	Non-Inverted Buck-Boost Converters with Dual Delta Sigma Modulators. IEEJ Transactions on Electronics, Information and Systems, 2009, 129, 153-158.	0.2	1
76	SAR ADC Algorithm With Redundancy Using Pseudo-Silver-Ratio. IEEJ Transactions on Electronics, Information and Systems, 2017, 137, 222-228.	0.2	1
77	Pass-Band Gain Improvement Technique for Passive RC Polyphase Filter in Bluetooth Low-IF Receiver Using Two RC Band-Stop Filters. Advanced Engineering Forum, 0, 38, 192-205.	0.3	1
78	Operation and Stability Analysis of Temperature-Insensitive MOS Reference Current Source with Self-Bias Circuit. , 2020, , .		1
79	Vision chip architecture with light adaptation mechanism. Artificial Life and Robotics, 1998, 2, 12-18.	1.2	0
80	Analysis of jitter accumulation in interleaved phase frequency detectors for high-accuracy on-chip jitter measurements. , 2011, , .		0
81	Background Self-Calibration Algorithm for Pipelined ADC Using Split ADC Scheme. IEICE Transactions on Electronics, 2011, E94-C, 1233-1236.	0.6	0
82	A reference-free on-chip timing jitter measurement circuit using self-referenced clock and a cascaded time difference amplifier in 65nm CMOS. , 2012, , .		0
83	A small, low power boost regulator optimized for energy harvesting applications. Analog Integrated Circuits and Signal Processing, 2013, 75, 207-216.	1.4	0
84	Analysis on a Cascaded Structure in Open-Loop Time Amplifier for High-Speed Operation. Key Engineering Materials, 2013, 596, 171-175.	0.4	0
85	Design Methodology and Jitter Analysis of a Delay Line for High-Accuracy On-Chip Jitter Measurements. Key Engineering Materials, 0, 596, 176-180.	0.4	0
86	Noise-Coupled Image Rejection Architecture of Complex Bandpass .DELTA..SIGMA.AD Modulator. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2010, E93-A, 390-394.	0.3	0
87	Stochastic TDC Architecture with Self-Calibration and its RTL Verification. IEEJ Transactions on Electronics, Information and Systems, 2017, 137, 335-341.	0.2	0
88	Consideration on Input Signal for ADC Histogram Test in Short Time. Advanced Engineering Forum, 0, 38, 83-92.	0.3	0
89	Classical Mathematics and Analog/Mixed-Signal IC Design. , 2021, , .		0
90	Innovative Practices Track: Innovative Analog Circuit Testing Technologies. , 2022, , .		0