Jong-Hyeok Yoon

List of Publications by Year
in descending order

13	127	1478505 6	1281871 11
papers	citations	h-index	g-index

13	13	13	136
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	A 40-nm, 64-Kb, 56.67 TOPS/W Voltage-Sensing Computing-In-Memory/Digital RRAM Macro Supporting Iterative Write With Verification and Online Read-Disturb Detection. IEEE Journal of Solid-State Circuits, 2022, 57, 68-79.	5.4	24
2	BitS-Net: Bit-Sparse Deep Neural Network for Energy-Efficient RRAM-Based Compute-In-Memory. IEEE Transactions on Circuits and Systems I: Regular Papers, 2022, 69, 1952-1961.	5.4	4
3	A 40-nm 118.44-TOPS/W Voltage-Sensing Compute-in-Memory RRAM Macro With Write Verification and Multi-Bit Encoding. IEEE Journal of Solid-State Circuits, 2022, 57, 845-857.	5.4	22
4	NeuroSLAM: A 65-nm 7.25-to-8.79-TOPS/W Mixed-Signal Oscillator-Based SLAM Accelerator for Edge Robotics. IEEE Journal of Solid-State Circuits, 2021, 56, 66-78.	5.4	11
5	A Framed-Pulsewidth Modulation Transceiver for High-Speed Broadband Communication Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2825-2835.	5.4	1
6	3.125-to-28.125 Gb/s 4.72 mW/Gb/s Multi- Standard Parallel Transceiver Supporting Channel-Independent Operation in 40-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers, 2020, 67, 2647-2658.	5.4	4
7	An Electronic Dispersion Compensation Transceiver for 10- and 28-Gb/s Directly Modulated Lasers-Based Optical Links. IEEE Journal of Solid-State Circuits, 2019, 54, 55-64.	5.4	1
8	A 3.125-to-28.125 Gb/s multi-standard transceiver with a fully channel-independent operation in 40nm CMOS. , 2018, , .		1
9	A 20Gb/s transceiver with framed-pulsewidth modulation in 40nm CMOS. , 2018, , .		6
10	A DC-to-12.5 Gb/s 9.76 mW/Gb/s All-Rate CDR With a Single <italic>LC</italic> VCO in 90 nm CMOS. IEEE Journal of Solid-State Circuits, 2017, 52, 856-866.	5.4	14
11	A 4 x 10-Gb/s Referenceless-and-Masterless Phase Rotator-Based Parallel Transceiver in 90-nm CMOS. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2015, , 1-11.	3.1	3
12	A 0.87 W Transceiver IC for 100 Gigabit Ethernet in 40 nm CMOS. IEEE Journal of Solid-State Circuits, 2015, 50, 399-413.	5.4	26
13	A 10-Gb/s CDR With an Adaptive Optimum Loop-Bandwidth Calibrator for Serial Communication Links. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2466-2472.	5.4	10