Mary Jane Irwin

List of Publications by Year
in descending order

35 papers	341 citations	1162889 8 h-index	940416 16 g-index
35 all docs	35 docs citations	35 times ranked	264 citing authors

#	Article	IF	Citations
1	Toward Increasing FPGA Lifetime. IEEE Transactions on Dependable and Secure Computing, 2008, 5, 115-127.	3.7	73
2	Design Space Exploration for 3-D Cache. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 444-455.	2.1	66
3	A helper thread based EDP reduction scheme for adapting application execution in CMPs. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	27
4	Designs of emerging memory based non-volatile TCAM for Internet-of-Things (IoT) and big-data processing: A 5T2R universal cell. , 2016, , .		23
5	The Arithmetic Cube. IEEE Transactions on Computers, 1987, C-36, 1342-1348.	2.4	21
6	Process-Variation-Aware Adaptive Cache Architecture and Management. IEEE Transactions on Computers, 2009, 58, 865-877.	2.4	20
7	A Parallel ASIC Architecture for Efficient Fractal Image Coding. Journal of Signal Processing Systems, 1998, 19, 97-113.	1.0	12
8	Compiler-directed proactive power management for networks. , 2005, , .		11
9	Reducing NoC energy consumption through compiler-directed channel voltage scaling. ACM SIGPLAN Notices, 2006, 41, 193-203.	0.2	8
10	Using Data Compression for Increasing Memory System Utilization. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009, 28, 901-914.	1.9	8
11	Design of energyâ€efficient circuits and systems using tunnel field effect transistors. IET Circuits, Devices and Systems, 2013, 7, 294-303.	0.9	8
12	Exploring heterogeneous NoC design space. , 2011, , .		7
13	Power-Area Trade-Offs in Divided Word Line Memory Arrays. Journal of Circuits, Systems and Computers, 1997, 07, 49-67.	1.0	6
14	Variation-Aware Low-Power Buffer Design. Conference Record of the Asilomar Conference on Signals, Systems and Computers, 2007, , .	0.0	6
15	Load Miss Prediction - Exploiting Power Performance Trade-offs. , 2007, , .		6
16	Energy-performance trade-offs for spatial access methods on memory-resident data. VLDB Journal, 2002, 11, 179-197.	2.7	5
17	Total Power Optimization for Combinational Logic Using Genetic Algorithms. Journal of Signal Processing Systems, 2010, 58, 145-160.	1.4	5
18	Investigating Simple Low Latency Reliable Multiported Register Files. , 2007, , .		4

#	Article	IF	Citations
19	A rational arithmetic processor. , 1981, , .		3
20	Analysis and solutions to issue queue process variation. , 2008, , .		3
21	Evaluating the role of scratchpad memories in chip multiprocessors for sparse matrix computations. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	3
22	Optimizing power and performance for reliable on-chip networks. , 2010, , .		3
23	Optimizing Leakage Energy Consumption in Cache Bitlines. Design Automation for Embedded Systems, 2004, 9, 5-18.	0.7	2
24	A Real Time Embedded Face Detector on FPGA. , 2006, , .		2
25	Exploring performance-power tradeoffs in providing reliability for NoC-based MPSoCs. , 2011, , .		2
26	Traffic steering between a low-latency unswitched TL ring and a high-throughput switched on-chip interconnect. , 2013, , .		2
27	An optimal time multiplication free algorithm for edge detection on a mesh. Journal of Signal Processing Systems, 1996, 13, 67-75.	1.0	1
28	Aggressive Dynamic Execution of Decoded Traces. Journal of Signal Processing Systems, 1999, 22, 65-75.	1.0	1
29	Memory Optimizations For Fast Power-Aware Sparse Computations. , 2007, , .		1
30	T-NUCA - a novel approach to non-uniform access latency cache architectures for 3D CMPs. , 2010, , .		1
31	An FPGA-based accelerator for cortical object classification. , 2012, , .		1
32	Numerical limitations on the design of digit online networks. , 1983, , .		0
33	Power efficient adaptive M-QAM design using adaptive pipelined analog-to-digital converter. , 2002, , .		0
34	Managing power, performance and reliability trade-offs. Parallel and Distributed Processing Symposium (IPDPS), Proceedings of the International Conference on, 2008, , .	1.0	0
35	Power and area reduction using carbon nanotube bundle interconnect in global clock tree distribution network. , 2009, , .		0