Yusuke Matsunaga

List of Publications by Year
in descending order

Source: https://exaly.com/author-pdf/11352327/publications.pdf

Version: 2024-02-01

11	37	2258059	2053705
papers	citations	3 h-index	5 g-index

11	11	11	8
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	An Exact Approach for GPC-Based Compressor Tree Synthesis. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2013, E96.A, 2553-2560.	0.3	11
2	Power and delay aware synthesis of multi-operand adders targeting LUT-based FPGAs. , 2011, , .		8
3	Multi-Operand Adder Synthesis Targeting FPGAs. IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences, 2011, E94-A, 2579-2586.	0.3	8
4	Area Recovery under Depth Constraint for Technology Mapping for LUT-based FPGAs. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 200-211.	0.8	3
5	Synthesis of parallel prefix adders considering switching activities. , 2008, , .		2
6	Efficient Fault Simulation Algorithms for Analyzing Soft Error Propagation in Sequential Circuits. IPSJ Transactions on System LSI Design Methodology, 2013, 6, 127-134.	0.8	2
7	An efficient performance improvement method utilizing specialized functional units in Behavioral Synthesis. , 2008, , .		1
8	A Soft Error Tolerance Estimation Method for Sequential Circuits. , 2011, , .		1
9	An Exact Estimation Algorithm of Error Propagation Probability for Sequential Circuits. IPSJ Transactions on System LSI Design Methodology, 2012, 5, 63-70.	0.8	1
10	Binding Refinement for Multiplexer Reduction. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 43-52.	0.8	0
11	Framework for Parallel Prefix Adder Synthesis Considering Switching Activities. IPSJ Transactions on System LSI Design Methodology, 2009, 2, 212-221.	0.8	0