Mohab Anis

List of Publications by Year
in descending order

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42	480	933447 10	794594 19
papers	citations	h-index	g-index

42	42	42	378
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Hotspot detection using machine learning. , 2016, , .		11
2	Model-Based Initial Bias (MIB): Toward a Single-Iteration Optical Proximity Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016, 35, 1630-1639.	2.7	2
3	Negative capacitance circuits for process variations compensation and timing yield improvement. , 2014, , .		0
4	Negative capacitance circuits for process variations compensation and timing yield improvement. , 2013, , .		0
5	Statistical SRAM Read Access Yield Improvement Using Negative Capacitance Circuits. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 92-101.	3.1	8
6	NBTI and Process Variations Compensation Circuits Using Adaptive Body Bias. IEEE Transactions on Semiconductor Manufacturing, 2012, 25, 460-467.	1.7	39
7	Power Supply Pads Assignment for Maximum Timing Yield. IEEE Transactions on Circuits and Systems II: Express Briefs, 2011, 58, 697-701.	3.0	3
8	Adaptive Body Bias for Reducing the Impacts of NBTI and Process Variations on 6T SRAM Cells. IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 2859-2871.	5.4	67
9	IR-Drop Aware Clustering Technique for Robust Power Grid in FPGAs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2011, 19, 1181-1191.	3.1	4
10	Guest Editorial Special Section on 2010 IEEE Custom Integrated Circuits Conference (CICC 2010). IEEE Transactions on Circuits and Systems I: Regular Papers, 2011, 58, 1993-1995.	5.4	0
11	Statistical timing yield improvement of dynamic circuits using negative capacitance technique. , 2010, , .		5
12	Comparative analysis of power yield improvement under process variation of sub-threshold flip-flops. , 2010, , .		2
13	Robust FPGA Design under Variations. , 2010, , .		1
14	Statistical Design of the 6T SRAM Bit Cell. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 93-104.	5.4	54
15	Statistical Approach for Yield Optimization for Minimum Energy Operation in Subthreshold Circuits Considering Variability Issues. IEEE Transactions on Semiconductor Manufacturing, 2010, 23, 77-86.	1.7	3
16	Scaling analysis of yield optimization considering supply and threshold voltage variations. , 2010, , .		1
17	FPGA Design for Timing Yield Under Process Variations. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 423-435.	3.1	17
18	Reducing SRAM Power Using Fine-Grained Wordline Pulsewidth Control. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 356-364.	3.1	12

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19	IR-Drop Management in FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 988-993.	2.7	4
20	A Power-Efficient Multipin ILP-Based Routing Technique. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 225-235.	5.4	6
21	A Design-Oriented Soft Error Rate Variation Model Accounting for Both Die-to-Die and Within-Die Variations in Submicrometer CMOS SRAM Cells. IEEE Transactions on Circuits and Systems I: Regular Papers, 2010, 57, 1298-1311.	5.4	25
22	Comparative Analysis of Timing Yield Improvement under Process Variations of Flip-Flops Circuits. , 2009, , .		19
23	Total Power Modeling in FPGAs Under Spatial Correlation. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 578-582.	3.1	7
24	Variability-Aware Bulk-MOS Device Design. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 205-216.	2.7	10
25	Design-Specific Optimization Considering Supply and Threshold Voltage Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1891-1901.	2.7	10
26	A Statistical Design-Oriented Delay Variation Model Accounting for Within-Die Variations. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1983-1995.	2.7	39
27	Statistical Thermal Profile Considering Process Variations: Analysis and Applications. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1027-1040.	2.7	33
28	Input Vector Reordering for Leakage Power Reduction in FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1555-1564.	2.7	7
29	A Comparative Study Between Static and Dynamic Sleep Signal Generation Techniques for Leakage Tolerant Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2008, 16, 1114-1126.	3.1	11
30	A robust single supply voltage SRAM read assist technique using selective precharge. , 2008, , .		6
31	Switching activity reduction in low power Booth multiplier. , 2008, , .		5
32	Variability-aware design of subthreshold devices. , 2008, , .		7
33	Advanced IC technology - opportunities and challenges. , 2008, , .		1
34	Area/yield trade-offs in scaled CMOS SRAM cell. , 2008, , .		0
35	A Timing-Driven Algorithm for Leakage Reduction in MTCMOS FPGAs. , 2007, , .		4
36	Variability in VLSI Circuits: Sources and Design Considerations. , 2007, , .		20

#	Article	IF	Citations
37	A Dual-Threshold FPGA Routing Design for Subthreshold Leakage Reduction. , 2007, , .		2
38	A Low-Power Multi-Pin Maze Routing Methodology. , 2007, , .		1
39	Dual-Threshold CAD Framework for Subthreshold Leakage Power Aware FPGAs. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 53-66.	2.7	6
40	Impact of technology scaling on leakage reduction techniques. , 2007, , .		5
41	Design-specific supply and threshold voltage optimization in nanometer era. Midwest Symposium on Circuits and Systems, 2007, , .	1.0	0
42	Dynamic Standby Prediction for Leakage Tolerant Microprocessor Functional Units. , 2006, , .		23