Yuanzhong Zhou

List of Publications by Year in descending order

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1307594 1125743 30 197 7 13 citations g-index h-index papers 30 30 30 97 docs citations times ranked citing authors all docs

#	Article	IF	CITATIONS
1	High-Robustness and Low-Capacitance Silicon-Controlled Rectifier for High-Speed I/O ESD Protection. IEEE Electron Device Letters, 2013, 34, 178-180.	3.9	40
2	Modeling and Simulation of Comprehensive Diode Behavior Under Electrostatic Discharge Stresses. IEEE Transactions on Device and Materials Reliability, 2019, 19, 90-96.	2.0	18
3	Compact Thermal Failure Model for Devices Subject to Electrostatic Discharge Stresses. IEEE Transactions on Electron Devices, 2015, 62, 4128-4134.	3.0	17
4	Prediction and Modeling of Thin Gate Oxide Breakdown Subject to Arbitrary Transient Stresses. IEEE Transactions on Electron Devices, 2010, 57, 2296-2305.	3.0	16
5	Gate oxide evaluation under very fast transmission line pulse (VFTLP) CDM-type stress. , 2008, , .		12
6	Optimizing high efficient plasma immersion ion implantation hydrogenation for poly-Si thin film transistors. Nuclear Instruments & Methods in Physics Research B, 1997, 124, 69-75.	1.4	10
7	ESD protection structure with reduced capacitance and overshoot voltage for high speed interface applications. Microelectronics Reliability, 2017, 79, 201-205.	1.7	10
8	Compact failure modeling for devices subject to electrostatic discharge stresses – A review pertinent to CMOS reliability simulation. Microelectronics Reliability, 2015, 55, 15-23.	1.7	9
9	Fabrication of low dielectric constant materials for ULSI multilevel interconnection by plasma ion implantation. IEEE Electron Device Letters, 1998, 19, 420-422.	3.9	8
10	ESD Simulation using Compact Models: from I/O Cell to Full Chip. , 2007, , .		8
10	ESD Simulation using Compact Models: from I/O Cell to Full Chip. , 2007, , . Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models. , 2006, , .		7
		3.0	
11	Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models., 2006,,. Plasma ion implantation hydrogenation of poly-Si CMOS thin-film transistors at low energy and high dose rate using an inductively-coupled plasma source. IEEE Transactions on Electron Devices, 1998, 45,	3.0	7
11 12	Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models., 2006,,. Plasma ion implantation hydrogenation of poly-Si CMOS thin-film transistors at low energy and high dose rate using an inductively-coupled plasma source. IEEE Transactions on Electron Devices, 1998, 45, 1324-1328. Modeling of high voltage devices for ESD event simulation in SPICE. Microelectronics Journal, 2012,		6
11 12 13	Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models., 2006,,. Plasma ion implantation hydrogenation of poly-Si CMOS thin-film transistors at low energy and high dose rate using an inductively-coupled plasma source. IEEE Transactions on Electron Devices, 1998, 45, 1324-1328. Modeling of high voltage devices for ESD event simulation in SPICE. Microelectronics Journal, 2012, 43, 305-311. Short-Time Hydrogen Passivation of Poly-Si CMOS Thin film Transistors by High Dose Rate Plasma Ion	2.0	6
11 12 13	Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models., 2006,,. Plasma ion implantation hydrogenation of poly-Si CMOS thin-film transistors at low energy and high dose rate using an inductively-coupled plasma source. IEEE Transactions on Electron Devices, 1998, 45, 1324-1328. Modeling of high voltage devices for ESD event simulation in SPICE. Microelectronics Journal, 2012, 43, 305-311. Short-Time Hydrogen Passivation of Poly-Si CMOS Thin film Transistors by High Dose Rate Plasma Ion Implantation. Materials Research Society Symposia Proceedings, 1995, 396, 515. N-Type Doping by Plasma Ion Implantation Using a PH ₃ SDS System. Materials Research	2.0	7664
11 12 13 14	Compact Modeling of On-Chip ESD Protection Using Standard MOS and BJT Models., 2006, , . Plasma ion implantation hydrogenation of poly-Si CMOS thin-film transistors at low energy and high dose rate using an inductively-coupled plasma source. IEEE Transactions on Electron Devices, 1998, 45, 1324-1328. Modeling of high voltage devices for ESD event simulation in SPICE. Microelectronics Journal, 2012, 43, 305-311. Short-Time Hydrogen Passivation of Poly-Si CMOS Thin film Transistors by High Dose Rate Plasma Ion Implantation. Materials Research Society Symposia Proceedings, 1995, 396, 515. N-Type Doping by Plasma Ion Implantation Using a PH < sub>3 < /sub> SDS System. Materials Research Society Symposia Proceedings, 1996, 438, 351.	2.0	7 6 4 4

#	Article	IF	CITATIONS
19	Plasma Immersion Ion Implantation Modification of Surface Properties of Polymer Material. Materials Research Society Symposia Proceedings, 1996, 438, 511.	0.1	3
20	vfTLP-VTH: A new method for quantifying the effectiveness of ESD protection for the CDM classification test. Microelectronics Reliability, 2013, 53, 196-204.	1.7	3
21	Plasma Ion Implantation for Flat Panel Displays. Materials Research Society Symposia Proceedings, 1996, 438, 321.	0.1	2
22	Investigations of Plasma Immersion Ion Implantation Hydrogenation for Poly-Si Tfts Using an Inductively Coupled Plasma Source. Materials Research Society Symposia Proceedings, 1996, 438, 357.	0.1	1
23	Plasma Chemistry Study of Plasma Ion Implantation Doping for Cmos Devices. Materials Research Society Symposia Proceedings, 1998, 510, 239.	0.1	1
24	Thermal failure and voltage overshoot models for diode behavior under electrostatic discharge stresses. , $2018, , .$		1
25	Nitrogen Plasma Ion Implantation into Carbon Films Deposited by the Anodic Vacuum ARc. Materials Research Society Symposia Proceedings, 1995, 388, 281.	0.1	O
26	Anodic vacuum arc deposition of carbon and nitrogen containing carbon films. , 0, , .		0
27	Investigations of Plasma Immersion Ion Implantation Hydrogenation for Poly-Si Tfts Using an Inductively Coupled Plasma Source. Materials Research Society Symposia Proceedings, 1996, 439, 269.	0.1	O
28	Study of high efficient Plasma Immersion Ion Implantation hydrogenation for CMOS poly-Si TFTs using an ICP plasma source. , 0, , .		0
29	Hydrodynamic and analytical models for plasma immersion ion implantation with dielectric substrates., 0, , .		0
30	Low-Dielectric Constant SiO(F,C) Films for ULSI Interconnections Prepared by CF4 Plasma Ion Implantation. Materials Research Society Symposia Proceedings, 1998, 511, 63.	0.1	0