George Theodoridis

List of Publications by Year
in descending order

16 papers	130 citations	1684188 5 h-index	1474206 9 g-index
16 all docs	16 docs citations	16 times ranked	142 citing authors

#	Article	IF	Citations
1	A High Performance Bitplane Encoder for the CCSDS 122.0-B-1 Compression Standard. , 2018, , .		0
2	High speed binary counter based on 1D Cellular Automata. , 2016, , .		3
3	Design and implementation of totally-self checking SHA-1 and SHA-256 hash functionsâ€™ architectures. Microprocessors and Microsystems, 2016, 45, 227-240.	2.8	22
4	Optimising the SHAâ€512 cryptographic hash function on FPGAs. IET Computers and Digital Techniques, 2014, 8, 70-82.	1.2	14
5	A Hybrid ILP-CP Model for Mapping Directed Acyclic Task Graphs to Multicore Architectures. , 2014, , .		4
6	An 8K-UHD capable 8-stage pipeline deblocking filter for H.264/AVC. , 2014, , .		1
7	A hardware implementation of the JVT Rate Control for H.264. , 2014, , .		0
8	Highâ€performance FPGA implementations of the cryptographic hash function JH. IET Computers and Digital Techniques, 2013, 7, 29-40.	1.2	1
9	A SYSTEMATIC FLOW FOR DEVELOPING TOTALLY SELF-CHECKING ARCHITECTURES FOR SHA-1 AND SHA-2 CRYPTOGRAPHIC HASH FAMILIES. Journal of Circuits, Systems and Computers, 2013, 22, 1350049.	1.5	2
10	On the exploitation of a high-throughput SHA-256 FPGA design for HMAC. ACM Transactions on Reconfigurable Technology and Systems, 2012, 5, 1-28.	2.5	34
11	A high throughput pipelined architecture for H.264/AVC deblocking filter. , 2010, , .		2
12	The ARISE Approach for Extending Embedded Processors With Arbitrary Hardware Accelerators. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 221-233.	3.1	15
13	An Application Development Framework for ARISE Reconfigurable Processors. ACM Transactions on Reconfigurable Technology and Systems, 2009, 2, 1-30.	2.5	4
14	The ARISE Reconfigurable Instruction Set Extensions Framework. , 2007, , .		4
15	High-Speed FPGA Implementation of Secure Hash Algorithm for IPSec and VPN Applications. Journal of Supercomputing, 2006, 37, 179-195.	3.6	19
16	A method for partitioning applications in hybrid reconfigurable architectures. Design Automation for Embedded Systems, 2005, 10, 27-47.	1.0	5