

# Saheli Sarkhel

## List of Publications by Year in descending order

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26  
papers

211  
citations

1307594

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h-index

1281871

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g-index

26  
all docs

26  
docs citations

26  
times ranked

103  
citing authors

#	ARTICLE	IF	CITATIONS
1	Statistical Analysis of a Low Power Analog Current Source. , 2022, , .		0
2	A 0.6 V 1.6 nA Constant Current Reference Circuit with Improved Power Supply Sensitivity. , 2021, , .		2
3	Analytical Model of a Strain Induced Lateral Channel Workfunction Engineered Surrounding Gate MOSFET. , 2020, , .		0
4	Exploring the Threshold Voltage Characteristics and Short Channel Behavior of Gate Engineered Front Gate Stack MOSFET with Graded Channel. Silicon, 2019, 11, 1421-1428.	3.3	0
5	Two-Dimensional Potential and Threshold Voltage Modeling of Work Function Engineered Double Gate High-k Gate Stack Schottky Barrier MOSFET. Journal of Electronic Materials, 2019, 48, 3823-3832.	2.2	5
6	3D Modelling and Performance Analysis of Dual Material Tri-Gate Tunnel Field Effect Transistor. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2019, 36, 117-129.	3.2	12
7	Analytical Modeling and Performance Characterization of a Double Gate MOSFET with Dielectric Pockets Incorporating Work Function Engineered Binary Metal Alloy Gate Electrode for Subdued SCEs. IETE Technical Review (Institution of Electronics and Telecommunication Engineers, India), 2018, 35, 506-513.	3.2	2
8	Two Dimensional Analytical Modeling based Threshold Voltage Characteristics of Proposed Linearly Graded Work Function Engineered Gate all around SB MOSFET. , 2018, , .		1
9	3D Modeling based Performance Analysis of Gate Engineered Trigate SON TFET with SiO <sub>2</sub> /HfO <sub>2</sub> stacked gate oxide. , 2018, , .		4
10	Compact 2D threshold voltage modeling and performance analysis of ternary metal alloy work-function-engineered double-gate MOSFET. Journal of Computational Electronics, 2017, 16, 648-657.	2.5	12
11	A compact analytical model of binary metal alloy silicon-on-nothing (BMASON) tunnel FET with interface trapped charges. Journal of Computational Electronics, 2017, 16, 704-713.	2.5	8
12	Parasitic fringe capacitance modeling of work function engineered double gate TFET. , 2017, , .		0
13	Analytical model for $I_{D<inf>D</inf>-V_{D<inf>D</inf>}$ characteristics of a triple metal double gate TFET. , 2016, , .		1
14	Exploring the Asymmetric Characteristics of a Double Gate MOSFET with Linearly Graded Binary Metal Alloy Gate Electrode for Enhanced Performance. IETE Journal of Research, 2016, 62, 786-794.	2.6	3
15	Compact 2D modeling and drain current performance analysis of a work function engineered double gate tunnel field effect transistor. Journal of Computational Electronics, 2016, 15, 104-114.	2.5	32
16	Recent research trends in gate engineered tunnel FET for improved current behavior by subduing the ambipolar effects: A review. , 2015, , .		17
17	A compact quasi 3D threshold voltage modeling and performance analysis of a novel linearly graded binary metal alloy quadruple gate MOSFET for subdued short channel effects. Superlattices and Microstructures, 2015, 82, 293-302.	3.1	19
18	A comprehensive two dimensional analytical study of a nanoscale linearly graded binary metal alloy gate cylindrical junctionless MOSFET for improved short channel performance. Journal of Computational Electronics, 2014, 13, 925-932.	2.5	10

#	ARTICLE	IF	CITATIONS
19	A compact capacitive approach based threshold voltage modeling and performance comparison of a novel UBR MOSFET with SOI MOSFET. , 2014, , .		0
20	Analytical modeling and simulation of a linearly graded binary metal alloy gate nanoscale cylindrical MOSFET for reduced short channel effects. Journal of Computational Electronics, 2014, 13, 599-605.	2.5	10
21	Study of power dissipation and delay of TWO dimensional SOI and SON based MOSFET inverter. , 2013, , .		1
22	Realization of gate performance using hybrid SET-CMOS pass transistor based logic gate. , 2013, , .		1
23	Analytical potential distribution model of symmetric double gate underlap MOSFET with binary metal alloy as gate electrode for subdued sces. , 2013, , .		1
24	Spatial Composition Grading of Binary Metal Alloy Gate Electrode for Short-Channel SOI/SON MOSFET Application. IEEE Transactions on Electron Devices, 2012, 59, 3280-3287.	3.0	67
25	A two dimensional analytical modeling of fully depleted dual material gate SON MOSFET and evidence for suppressed SCEs. , 2012, , .		3
26	Small - signal parameter extraction to study the RF performance of SOI and SON MOSFET. , 2012, , .		0