Rance Rodrigues

List of Publications by Year
in descending order

18	156	2682572	2550090
papers	citations	2	3
		h-index	g-index

18	18	18	128
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Does the Sharing of Execution Units Improve Performance/Power of Multicores?. Transactions on Embedded Computing Systems, 2015, 14, 1-24.	2.9	2
2	Performance and Power Benefits of Sharing Execution Units between a High Performance Core and a Low Power Core. , 2014, , .		5
3	A unified view of non-monotonic core selection and application steering in heterogeneous chip multiprocessors. , 2013, , .		3
4	A Study on the Use of Performance Counters to Estimate Power in Microprocessors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 882-886.	3.0	53
5	A low power architecture for online detection of execution errors in SMT processors. , 2013, , .		4
6	A study on polymorphing superscalar processor dynamically to improve power efficiency. , 2013, , .		2
7	Improving performance per watt of asymmetric multi-core processors via online program phase classification and adaptive core morphing. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-23.	2.6	15
8	A mechanism to verify cache coherence transactions in multicore systems. , 2012, , .		1
9	Scalable Thread Scheduling in Asymmetric Multicores for Power Efficiency. , 2012, , .		12
10	Dynamic Thread Scheduling in Asymmetric Multicores to Maximize Performance-per-Watt. , 2012, , .		9
11	On graceful degradation of chip multiprocessors in presence of faults via flexible pooling of critical execution units. , 2011, , .		5
12	Performance Per Watt Benefits of Dynamic Core Morphing in Asymmetric Multicores. , 2011, , .		32
13	Model based double patterning lithography (DPL) and simulated annealing (SA). , 2011, , .		0
14	An Architecture to Enable Life Cycle Testing in CMPs. , 2011, , .		5
15	On graceful degradation of microprocessors in presence of faults via resource banking. , 2011, , .		0
16	An Architecture to Enable Lifetime Full Chip Testability in Chip Multiprocessors. , 2011, , .		0
17	A study on performance benefits of core morphing in an asymmetric multicore processor. , 2010, , .		3
18	Shadow checker (SC): A low-cost hardware scheme for online detection of faults in small memory structures of a microprocessor. , 2010, , .		5