Rance Rodrigues

List of Publications by Year
in descending order

18 papers	156 citations	2682572 2 h-index	2550090 3 g-index
18 all docs	18 docs citations	18 times ranked	128 citing authors

#	Article	IF	Citations
1	A Study on the Use of Performance Counters to Estimate Power in Microprocessors. IEEE Transactions on Circuits and Systems II: Express Briefs, 2013, 60, 882-886.	3.0	53
2	Performance Per Watt Benefits of Dynamic Core Morphing in Asymmetric Multicores. , 2011, , .		32
3	Improving performance per watt of asymmetric multi-core processors via online program phase classification and adaptive core morphing. ACM Transactions on Design Automation of Electronic Systems, 2013, 18, 1-23.	2.6	15
4	Scalable Thread Scheduling in Asymmetric Multicores for Power Efficiency. , 2012, , .		12
5	Dynamic Thread Scheduling in Asymmetric Multicores to Maximize Performance-per-Watt. , 2012, , .		9
6	Shadow checker (SC): A low-cost hardware scheme for online detection of faults in small memory structures of a microprocessor. , 2010, , .		5
7	On graceful degradation of chip multiprocessors in presence of faults via flexible pooling of critical execution units. , 2011, , .		5
8	An Architecture to Enable Life Cycle Testing in CMPs. , 2011, , .		5
9	Performance and Power Benefits of Sharing Execution Units between a High Performance Core and a Low Power Core. , 2014, , .		5
10	A low power architecture for online detection of execution errors in SMT processors. , 2013, , .		4
11	A study on performance benefits of core morphing in an asymmetric multicore processor. , 2010, , .		3
12	A unified view of non-monotonic core selection and application steering in heterogeneous chip multiprocessors. , 2013, , .		3
13	A study on polymorphing superscalar processor dynamically to improve power efficiency. , 2013, , .		2
14	Does the Sharing of Execution Units Improve Performance/Power of Multicores?. Transactions on Embedded Computing Systems, 2015, 14, 1-24.	2.9	2
15	A mechanism to verify cache coherence transactions in multicore systems. , 2012, , .		1
16	Model based double patterning lithography (DPL) and simulated annealing (SA). , 2011, , .		0
17	On graceful degradation of microprocessors in presence of faults via resource banking. , 2011, , .		0
18	An Architecture to Enable Lifetime Full Chip Testability in Chip Multiprocessors. , 2011, , .		0