Jun Lin

List of Publications by Year in Descending Order

89 papers	781 citations	15 h-index	23 g-index
127 ext. papers	1,106 ext. citations	2.9 avg, IF	4.95 L-index

#	Paper	IF	Citations
89	An Improved Reliability-Based Decoding Algorithm for NB-LDPC Codes. *IEEE Communications Letters*, **2021**, 25, 1153-1157	3.8	2
88	An Efficient and Flexible Accelerator Design for Sparse Convolutional Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 2936-2949	3.9	6
87	Low-Latency Hardware Accelerator for Improved Engle-Granger Cointegration in Pairs Trading. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 2911-2924	3.9	3
86	Counter Random Gradient Descent Bit-Flipping Decoder for LDPC Codes **2021**,		2
85	Evaluations on Deep Neural Networks Training Using Posit Number System. *IEEE Transactions on Computers*, **2021**, 70, 174-187	2.5	14
84	Design of High-Performance and Area-Efficient Decoder for 5G LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2021**, 68, 879-891	3.9	7
83	Efficient Software Implementation of the SIKE Protocol Using New Data Representation. *IEEE Transactions on Computers*, **2021**, 1-1	2.5	2
82	Fast Modular Multipliers for Supersingular Isogeny-Based Post-Quantum Cryptography. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2021**, 29, 359-371	2.6	2
81	A Precision-Scalable Energy-Efficient Convolutional Neural Network Accelerator. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2020**, 67, 3484-3497	3.9	7
80	Fine-Grained Bit-Flipping Decoding for LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 896-900	3.5	8
79	Efficient Precision-Adjustable Architecture for Softmax Function in Deep Learning. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 3382-3386	3.5	11
78	Multi-Layer Generalized Integrated Interleaved Codes. *IEEE Communications Letters*, **2020**, 24, 1880-1884	3.8	3
77	A Proximal Iteratively Reweighted Approach for Efficient Network Sparsification. *IEEE Transactions on Computers*, **2020**, 1-1	2.5	1
76	Hardware Accelerator for Multi-Head Attention and Position-Wise Feed-Forward in the Transformer **2020**,		6
75	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 1399-1403	3.5	2
74	Information Storage Bit-Flipping Decoder for LDPC Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2020**, 28, 2464-2468	2.6	5
73	Hardware Accelerator for Engle-Granger Cointegration in Pairs Trading **2020**,		1

72	Optimized Trellis-Based Min-Max Decoder for NB-LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2020**, 67, 57-61	3.5	5
71	USCA: A Unified Systolic Convolution Array Architecture for Accelerating Sparse Neural Network **2019**,		3
70	Efficient T-EMS Based Decoding Algorithms for High-Order LDPC Codes. *IEEE Access*, **2019**, 7, 50980-50992	3.5	1
69	Improved Fast-SSC-Flip Decoding of Polar Codes. *IEEE Communications Letters*, **2019**, 23, 950-953	3.8	6
68	A Low-latency Sparse-Winograd Accelerator for Convolutional Neural Networks **2019**,		8
67	Analysis and Design of a Large Dither Injection Circuit for Improving Linearity in Pipelined ADCs. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2019**, 27, 2008-2020	2.6	5
66	E-LSTM: An Efficient Hardware Architecture for Long Short-Term Memory. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, **2019**, 9, 280-291	5.2	16
65	A 124-Gb/s Decoder for Generalized Integrated Interleaved Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 3174-3187	3.9	10
64	An Improved Gradient Descent Bit-Flipping Decoder for LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 3188-3200	3.9	8
63	Modified GII-BCH Codes for Low-Complexity and Low-Latency Encoders. *IEEE Communications Letters*, **2019**, 23, 785-788	3.8	5
62	A High-Speed Successive-Cancellation Decoder for Polar Codes Using Approximate Computing. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 227-231	3.5	4
61	FPAP: A Folded Architecture for Energy-Quality Scalable Convolutional Neural Networks. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2019**, 66, 288-301	3.9	4
60	A New Clock Phase Calibration Method in High-Speed and High-Resolution DACs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 332-336	3.5	
59	An Efficient Post-Processor for Lowering the Error Floor of LDPC Codes. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 397-401	3.5	2
58	Background Calibration of Comparator Offsets in SHA-Less Pipelined ADCs. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2019**, 66, 357-361	3.5	3
57	A New Probabilistic Gradient Descent Bit Flipping Decoder for LDPC Codes **2019**,		4
56	Methodology for Efficient Reconfigurable Architecture of Generative Neural Network **2019**,		4
55	TIE **2019**,		19

54	A Novel Low-Complexity Joint Coding and Decoding Algorithm for NB-LDPC Codes **2019**,		1
53	A New Fast-SSC-Flip Decoding of Polar Codes **2019**,		1
52	A Hardware-Oriented and Memory-Efficient Method for CTC Decoding. *IEEE Access*, **2019**, 7, 120681-120694	3.3	3
51	Improved Soft-Assisted Iterative Bounded Distance Decoding for Product Codes **2019**,		1
50	DynExit: A Dynamic Early-Exit Strategy for Deep Residual Networks **2019**,		1
49	Ultra-Fast Modular Multiplication Implementation for Isogeny-Based Post-Quantum Cryptography **2019**,		6
48	Training Deep Neural Networks Using Posit Number System **2019**,		4
47	Hybrid Preconditioned CG Detection with Sequential Update for Massive MIMO Systems **2019**,		1
46	Hardware Implementation of Improved Fast-SSC-Flip Decoder for Polar Codes **2019**,		5
45	Fast-ABC: A Fast Architecture for Bottleneck-Like Based Convolutional Neural Networks **2019**,		4
44	An Improved Gauss-Seidel Algorithm and Its Efficient Architecture for Massive MIMO Systems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 1194-1198	3.5	22
43	Efficient Hardware Architectures for Deep Convolutional Neural Network. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2018**, 65, 1941-1953	3.9	61
42	Low Complexity Message Passing Detection Algorithm for Large-Scale MIMO Systems. *IEEE Wireless Communications Letters*, **2018**, 7, 708-711	5.9	19
41	A Stage-Combined Belief Propagation Decoder for Polar Codes. *Journal of Signal Processing Systems*, **2018**, 90, 687-694	1.4	0
40	A 21.66 Gbps Nonbinary LDPC Decoder for High-Speed Communications. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2018**, 65, 226-230	3.5	4
39	Hardware-Oriented Compression of Long Short-Term Memory for Efficient Inference. *IEEE Signal Processing Letters*, **2018**, 25, 984-988	3.2	6
38	Parameter-Free ell_p -Box Decoding of LDPC Codes. *IEEE Communications Letters*, **2018**, 22, 1318-1321	3.8	5
37	An Efficient Convolution Core Architecture for Privacy-Preserving Deep Learning **2018**,		6

36	FPAP: A Folded Architecture for Efficient Computing of Convolutional Neural Networks **2018**,		2
35	An Energy-Efficient Architecture for Binary Weight Convolutional Neural Networks. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2018**, 26, 280-293	2.6	34
34	A High-Speed and Low-Complexity Architecture for Softmax Function in Deep Learning **2018**,		25
33	A Low-Complexity Decoder for Turbo Product Codes Based on Extended Hamming Codes **2018**,		1
32	Comparison between Generalized Integrated Interleaved Codes and Generalized Error Location Codes **2018**,		1
31	Fast and Low-Complexity Decoding Algorithm and Architecture for Quadruple-Error-Correcting RS codes **2018**,		3
30	A Low-Complexity Massive MIMO Detection Algorithm Based on Matrix Partition **2018**,		2
29	A reduced complexity decoding algorithm for NB-LDPC codes **2017**,		2
28	An access pattern based adaptive mapping function for GPGPU scratchpad memory. *IEICE Electronics Express*, **2017**, 14, 20170373-20170373	0.5	
27	Optimized sorting network for successive cancellation list decoding of polar codes. *IEICE Electronics Express*, **2017**, 14, 20170735-20170735	0.5	3
26	Low-complexity detection algorithms based on matrix partition for massive MIMO **2017**,		4
25	Accelerating Recurrent Neural Networks: A Memory-Efficient Approach. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 2763-2775	2.6	39
24	Efficient Soft Cancelation Decoder Architectures for Polar Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2017**, 25, 87-99	2.6	11
23	Energy efficient SVM classifier using approximate computing **2017**,		4
22	Reduced complexity message passing detection algorithm in large-scale MIMO systems **2017**,		1
21	An ultra-long FFT architecture implemented in a reconfigurable application specified processor. *IEICE Electronics Express*, **2016**, 13, 20160504-20160504	0.5	5
20	Design and implementation of high performance matrix inversion based on reconfigurable processor. *IEICE Electronics Express*, **2016**, 13, 20160579-20160579	0.5	2
19	A high throughput belief propagation decoder architecture for polar codes **2016**,		3

18	Intra-layer nonuniform quantization of convolutional neural network **2016**,		5
17	Efficient convolution architectures for convolutional neural network **2016**,		13
16	A Multimode Area-Efficient SCL Polar Decoder. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2016**, 24, 3499-3512	2.6	18
15	A High Throughput List Decoder Architecture for Polar Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 1-14	2.6	15
14	A hybrid partial sum computation unit architecture for list decoders of polar codes **2015**,		1
13	Reduced complexity belief propagation decoders for polar codes **2015**,		14
12	An Efficient List Decoder Architecture for Polar Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2015**, 23, 2508-2518	2.6	35
11	Efficient Error Control Decoder Architectures for Noncoherent Random Linear Network Coding. *Journal of Signal Processing Systems*, **2014**, 76, 195-209	1.4	
10	Efficient list decoder architecture for polar codes **2014**,		20
9	. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2014**, 22, 2649-2660	2.6	11
8	A reduced latency list decoding algorithm for polar codes **2014**,		17
7	Efficient Shuffled Decoder Architecture for Nonbinary Quasi-Cyclic LDPC Codes. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, **2013**, 21, 1756-1761	2.6	15
6	Linearized Polynomial Interpolation and Its Applications. *IEEE Transactions on Signal Processing*, **2013**, 61, 206-217	4.8	7
5	Reduced-Complexity Decoders of Long Reed-Solomon Codes Based on Composite Cyclotomic Fourier Transforms. *IEEE Transactions on Signal Processing*, **2012**, 60, 3920-3925	4.8	6
4	Flexible LDPC Decoder Design for Multigigabit-per-Second Applications. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 116-124	3.9	36
3	An Efficient VLSI Architecture for Nonbinary LDPC Decoders. *IEEE Transactions on Circuits and Systems II: Express Briefs*, **2010**, 57, 51-55	3.5	27
2	Efficient Decoder Design for Nonbinary Quasicyclic LDPC Codes. *IEEE Transactions on Circuits and Systems I: Regular Papers*, **2010**, 57, 1071-1082	3.9	46
1	LDPC decoder design for high rate wireless personal area networks. *IEEE Transactions on Consumer Electronics*, **2009**, 55, 455-460	4.8	5