Andrew B Kahng

List of Publications by Year
in descending order

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59	2,900	535685	355658
papers	citations	17 h-index	38 g-index

59	59	59	1790
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	PROBE2.0: A Systematic Framework for Routability Assessment From Technology to Design in Advanced Nodes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1495-1508.	1.9	7
2	TritonRoute-WXL: The Open-Source Router With Integrated DRC Engine. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2022, 41, 1076-1089.	1.9	7
3	Revisiting inherent noise floors for interconnect prediction. , 2020, , .		10
4	Enhancing sensitivity-based power reduction for an industry IC design context. The Integration VLSI Journal, 2019, 66, 96-111.	1.3	10
5	PROBE: A Placement, Routing, Back-End-of-Line Measurement Utility. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2018, 37, 1459-1472.	1.9	8
6	New directions for learning-based IC design tools and methodologies. , 2018, , .		28
7	Machine Learning Applications in Physical Design. , 2018, , .		60
8	INVITED: Reducing Time and Effort in IC Implementation: A Roadmap of Challenges and Solutions. , 2018, , .		3
9	Reducing time and effort in IC implementation: a roadmap of challenges and solutions. , 2018, , .		12
10	Benchmarking of Mask Fracturing Heuristics. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 170-183.	1.9	3
11	MILP-Based Optimization of 2-D Block Masks for Timing-Aware Dummy Segment Removal in Self-Aligned Multiple Patterning Layouts. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 1075-1088.	1.9	1
12	Adaptive Tuning of Photonic Devices in a Photonic NoC Through Dynamic Workload Allocation. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2017, 36, 801-814.	1.9	20
13	ORION3.0: A Comprehensive NoC Router Estimation Tool. IEEE Embedded Systems Letters, 2015, 7, 41-45.	1.3	83
14	Synthesis and Analysis of Design-Dependent Ring Oscillator (DDRO) Performance Monitors. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2014, 22, 2117-2130.	2.1	22
15	Toward Holistic Modeling, Margining and Tolerance of IC Variability. , 2014, , .		1
16	On Aging-Aware Signoff for Circuits With Adaptive Voltage Scaling. IEEE Transactions on Circuits and Systems I: Regular Papers, 2014, 61, 2920-2930.	3.5	9
17	Enhancing the Efficiency of Energy-Constrained DVFS Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2013, 21, 1769-1782.	2.1	35
18	Impact of Adaptive Voltage Scaling on Aging-Aware Signoff. , 2013, , .		9

#	Article	IF	Citations
19	Sensitivity-guided metaheuristics for accurate discrete gate sizing. , 2012, , .		54
20	ORION 2.0: A Power-Area Simulator for Interconnection Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 191-196.	2.1	218
21	Roads not taken. IEEE Design and Test of Computers, 2011, 28, 74-75.	1.4	2
22	The Future of Signoff. IEEE Design and Test of Computers, 2011, 28, 86-89.	1.4	1
23	Scaling: More than Moore's law. IEEE Design and Test of Computers, 2010, 27, 86-87.	1.4	49
24	Accurate Predictive Interconnect Modeling for System-Level Design. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2010, 18, 679-684.	2.1	10
25	Accurate Machine-Learning-Based On-Chip Router Modeling. IEEE Embedded Systems Letters, 2010, 2, 62-66.	1.3	36
26	Layout Decomposition Approaches for Double Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 939-952.	1.9	74
27	Timing Yield-Aware Color Reassignment and Detailed Placement Perturbation for Bimodal CD Distribution in Double Patterning Lithography. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2010, 29, 1229-1242.	1.9	16
28	Improved on-chip router analytical power and area modeling. , 2010, , .		19
29	Architectural-level prediction of interconnect wirelength and fanout. , 2009, , .		4
30	ORION 2.0: A fast and accurate NoC power and area model for early-stage design space exploration. , 2009, , .		456
31	CMP Fill Synthesis: A Survey of Recent Studies. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 3-19.	1.9	66
32	Fast Dual-Graph-Based Hotspot Filtering. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2008, 27, 1635-1642.	1.9	18
33	DOE-Based Extraction of CMP, Active and Via Fill Impact on Capacitances. IEEE Transactions on Semiconductor Manufacturing, 2008, 21, 22-32.	1.4	5
34	Fast and Efficient Bright-Field AAPSM Conflict Detection and Correction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 115-126.	1.9	13
35	Statistical Timing Analysis in the Presence of Signal-Integrity Effects. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2007, 26, 1873-1877.	1.9	11
36	Stochastic Power/Ground Supply Voltage Prediction and Optimization Via Analytical Placement. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2007, 15, 904-912.	2.1	6

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37	A DOE Set for Normalization-Based Extraction of Fill Impact on Capacitances. , 2007, , .		21
38	COMPUTER-AIDED OPTIMIZATION OF DNA ARRAY DESIGN AND MANUFACTURING. , 2006, , 235-269.		1
39	Interconnect Matching Design Rule Inferring and Optimization through Correlation Extraction. Proceedings - IEEE International Conference on Computer Design: VLSI in Computers and Processors, 2006, , .	0.0	0
40	Quantifying Error in Dynamic Power Estimation of CMOS Circuits. Analog Integrated Circuits and Signal Processing, 2005, 42, 253-264.	0.9	10
41	Routing-aware scan chain ordering. ACM Transactions on Design Automation of Electronic Systems, 2005, 10, 546-560.	1.9	17
42	APlace. , 2005, , .		52
43	Power-aware placement. , 2005, , .		94
44	Scalable Heuristics for Design of DNA Probe Arrays. Journal of Computational Biology, 2004, 11, 429-447.	0.8	10
45	Match twice and stitch: a new TSP tour construction heuristic. Operations Research Letters, 2004, 32, 499-509.	0.5	23
46	Design technology productivity in the DSM era (invited talk). , 2001, , .		7
47	On switch factor based analysis of coupled RC interconnects. , 2000, , .		85
48	Tuning Strategies for Global Interconnects in High-Performance Deep-Submicron ICs. VLSI Design, 1999, 10, 21-34.	0.5	17
49	Spectral partitioning with multiple eigenvectors. Discrete Applied Mathematics, 1999, 90, 3-26.	0.5	131
50	How to test a tree. Networks, 1998, 32, 189-197.	1.6	0
51	Robust IP watermarking methodologies for physical design. , 1998, , .		86
52	New efficient algorithms for computing effective capacitance. , 1998, , .		26
53	Improved Large-Step Markov Chain Variants for the Symmetric TSP. Journal of Heuristics, 1997, 3, 63-81.	1.1	28
54	OPTIMAL ALGORITHMS FOR SUBSTRATE TESTING IN MULTI-CHIP MODULES. Selected Topics in Electornics and Systems, 1996, , 181-198.	0.2	3

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55	OPTIMAL ALGORITHMS FOR SUBSTRATE TESTING IN MULTI-CHIP MODULES. International Journal of High Speed Electronics and Systems, 1995, 06, 595-612.	0.3	9
56	Old Bachelor Acceptance: A New Class of Non-Monotone Threshold Accepting Methods. ORSA Journal on Computing, 1995, 7, 417-425.	1.7	65
57	Recent directions in netlist partitioning: a survey. The Integration VLSI Journal, 1995, 19, 1-81.	1.3	494
58	A new adaptive multi-start technique for combinatorial global optimizations. Operations Research Letters, 1994, 16, 101-113.	0.5	312
59	Best-so-far vs. where-you-are: implications for optimal finite-time annealing. Systems and Control Letters, 1994, 22, 71-78.	1.3	23