

Aaron Thean

List of Publications by Year in descending order

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27
papers

400
citations

687220

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794469

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28
docs citations

28
times ranked

549
citing authors

#	ARTICLE	IF	CITATIONS
1	The effect of Ga pre-deposition on Si (111) surface for InAs nanowire selective area hetero-epitaxy. Journal of Applied Physics, 2018, 123, .	1.1	2
2	A New Quality Metric for IIIâ€V/High-k MOS Gate Stacks Based on the Frequency Dispersion of Accumulation Capacitance and the CET. IEEE Electron Device Letters, 2017, 38, 318-321.	2.2	11
3	On the distribution of oxide defect levels in Al ₂ O ₃ and HfO ₂ high-k dielectrics deposited on InGaAs metal-oxide-semiconductor devices studied by capacitance-voltage hysteresis. Journal of Applied Physics, 2017, 121, 144504.	1.1	13
4	Correlation between surface reconstruction and polytypism in InAs nanowire selective area epitaxy. Physical Review Materials, 2017, 1, .	0.9	10
5	Intrinsic Robustness of TFET Subthreshold Swing to Interface and Oxide Traps: A Comparative PBTI Study of InGaAs TFETs and MOSFETs. IEEE Electron Device Letters, 2016, 37, 1055-1058.	2.2	29
6	Impact of the low temperature operation on long channel strained Ge pFinFETs fabricated with STI first and last processes. , 2016, , .		2
7	Electric-field induced quantum broadening of the characteristic energy level of traps in semiconductors and oxides. Journal of Applied Physics, 2016, 120, .	1.1	9
8	GR-Noise Characterization of Ge pFinFETs With STI First and STI Last Processes. IEEE Electron Device Letters, 2016, 37, 1092-1095.	2.2	9
9	An Analytical Model of MOS Admittance for Border Trap Density Extraction in High- k Dielectrics of IIIâ€V MOS Devices. IEEE Transactions on Electron Devices, 2016, 63, 4707-4713.	1.6	6
10	Uniform Strain in Heterostructure Tunnel Field-Effect Transistors. IEEE Electron Device Letters, 2016, 37, 337-340.	2.2	23
11	Full-zone spectral envelope function formalism for the optimization of line and point tunnel field-effect transistors. Journal of Applied Physics, 2015, 118, .	1.1	13
12	Temperature dependence of frequency dispersion in IIIâ€V metal-oxide-semiconductor C-V and the capture/emission process of border traps. Applied Physics Letters, 2015, 107, .	1.5	25
13	Impact of starting measurement voltage relative to flat-band voltage position on the capacitance-voltage hysteresis and on the defect characterization of InGaAs/high-k metal-oxide-semiconductor stacks. Applied Physics Letters, 2015, 107, .	1.5	21
14	Record performance InGaAs homo-junction TFET with superior SS reliability over MOSFET. , 2015, , .		25
15	On MOS admittance modeling to study border trap capture/emission and its effect on electrical behavior of high-k/IIIâ€V MOS devices. Microelectronic Engineering, 2015, 147, 227-230.	1.1	6
16	Quantitative Method to Determine Planar Defect Frequency in InAs Nanowires by High Resolution X-ray Diffraction. Crystal Growth and Design, 2015, 15, 3868-3874.	1.4	4
17	Improved source design for p-type tunnel field-effect transistors: Towards truly complementary logic. Applied Physics Letters, 2014, 105, .	1.5	16
18	Bilayer Graphene Tunneling FET for Sub-0.2 V Digital CMOS Logic Applications. IEEE Electron Device Letters, 2014, 35, 1308-1310.	2.2	10

#	ARTICLE	IF	CITATIONS
19	Determination of energy and spatial distribution of oxide border traps in In _{0.53} Ga _{0.47} As MOS capacitors from capacitance–voltage characteristics measured at various temperatures. Microelectronics Reliability, 2014, 54, 746-754.	0.9	27
20	Fast Ramped Voltage Characterization of Single Trap Bias and Temperature Impact on Time-Dependent $I_{\text{on}}(V_{\text{TH}})$ Variability. IEEE Transactions on Electron Devices, 2014, 61, 3139-3144.	1.6	15
21	Superior Reliability of Junctionless pFinFETs by Reduced Oxide Electric Field. IEEE Electron Device Letters, 2014, 35, 1179-1181.	2.2	31
22	Chemically enhanced double-gate bilayer graphene field-effect transistor with neutral channel for logic applications. Nanotechnology, 2014, 25, 345203.	1.3	4
23	Quantum mechanical solver for confined heterostructure tunnel field-effect transistors. Journal of Applied Physics, 2014, 115, 053706.	1.1	20
24	Sidewall Crystalline Orientation Effect of Post-treatments for a Replacement Metal Gate Bulk Fin Field Effect Transistor. ACS Applied Materials & Interfaces, 2013, 5, 8865-8868.	4.0	15
25	1/f noise analysis of replacement metal gate bulk p-type fin field effect transistor. Applied Physics Letters, 2013, 102, 073503.	1.5	13
26	Plasma doping and reduced crystalline damage for conformally doped fin field effect transistors. Applied Physics Letters, 2013, 102, .	1.5	28
27	Low Frequency Noise Analysis for Post-Treatment of Replacement Metal Gate. IEEE Transactions on Electron Devices, 2013, 60, 2960-2962.	1.6	12