Bill Lin

List of Publications by Year
in descending order

46	465	1162889 8	996849 15
papers	citations	h-index	g-index

46	46	46	301
all docs	docs citations	times ranked	citing authors

#	Article	IF	Citations
1	Network optimization for unified packet and circuit switched networks. Optimization and Engineering, 2020, 21, 159-180.	1.3	2
2	Select to Better Learn: Fast and Accurate Deep Learning Using Data Selection From Nonlinear Manifolds. , 2020, , .		5
3	Efficient Traffic Load-Balancing via Incremental Expansion of Routing Choices. ACM Transactions on Modeling and Performance Evaluation of Computing Systems, 2019, 4, 1-35.	0.8	4
4	Uniform Minimal First: Latency Reduction in Throughput-Optimal Oblivious Routing for Mesh-Based Networks-on-Chip. IEEE Embedded Systems Letters, 2019, 11, 81-84.	1.3	8
5	Safe Randomized Load-Balanced Switching by Diffusing Extra Loads. Performance Evaluation Review, 2019, 46, 135-137.	0.4	0
6	Safe Randomized Load-Balanced Switching by Diffusing Extra Loads. , 2018, , .		0
7	Improving Backpressure-based Adaptive Routing via Incremental Expansion of Routing Choices. , 2017, , .		3
8	Safe Randomized Load-Balanced Switching By Diffusing Extra Loads. Proceedings of the ACM on Measurement and Analysis of Computing Systems, 2017, 1, 1-37.	1.4	7
9	Sharing a global on-chip transmission line medium without centralized scheduling. , 2016, , .		1
10	Safe Randomized Load-Balanced Switching by Diffusing Extra Loads. Performance Evaluation Review, 2016, 44, 397-398.	0.4	3
11	Sprinklers. , 2014, , .		7
12	Reservation-Based Packet Bufferswith Deterministic Packet Departures. IEEE Transactions on Parallel and Distributed Systems, 2014, 25, 1297-1305.	4.0	1
13	Per-Flow Queue Management with Succinct Priority Indexing Structures for High Speed Packet Scheduling. IEEE Transactions on Parallel and Distributed Systems, 2013, 24, 1380-1389.	4.0	4
14	Guest Editors' Introduction: Special Issue on Quality-of-Service. IEEE Transactions on Network and Service Management, 2013, 10, 1-2.	3.2	4
15	DRAM-Based Statistics Counter Array Architecture With Performance Guarantee. IEEE/ACM Transactions on Networking, 2012, 20, 1040-1053.	2.6	6
16	Distributed measurement-aware routing: Striking a balance between measurement and traffic engineering. , 2012, , .		1
17	Oblivious routing design for mesh networks to achieve a new worst-case throughput bound. , 2012, , .		2
18	Robust Pipelined Memory System with Worst Case Performance Guarantee for Network Processing. IEEE Transactions on Computers, 2012, 61, 1386-1400.	2.4	3

#	Article	IF	Citations
19	Randomized Partially-Minimal Routing: Near-Optimal Oblivious Routing for 3-D Mesh Networks. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2012, 20, 2080-2093.	2.1	3
20	Per-flow Queue Scheduling with Pipelined Counting Priority Index. , 2011, , .		1
21	Extending the Effective Throughput of NoCs With Distributed Shared-Buffer Routers. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2011, 30, 548-561.	1.9	18
22	Designing efficient codes for synchronization error channels. , 2011, , .		1
23	The taming of the shrew: mitigating low-rate TCP-targeted attack. IEEE Transactions on Network and Service Management, 2010, 7, 1-13.	3.2	19
24	Birkhoff-von Neumann switching with statistical traffic profiles. Computer Communications, 2010, 33, 848-851.	3.1	1
25	Block-based packet buffer with deterministic packet departures. , 2010, , .		6
26	Accurate Machine-Learning-Based On-Chip Router Modeling. IEEE Embedded Systems Letters, 2010, 2, 62-66.	1.3	36
27	Design of a High-Throughput Distributed Shared-Buffer NoC Router. , 2010, , .		54
28	Improved on-chip router analytical power and area modeling. , 2010, , .		19
29	The Concurrent Matching Switch Architecture. IEEE/ACM Transactions on Networking, 2010, 18, 1330-1343.	2.6	19
30	Design and Analysis of a Robust Pipelined Memory System. , 2010, , .		9
31	Design and performance analysis of a DRAM-based statistics counter array architecture. , 2009, , .		12
32	The interleaved matching switch architecture. IEEE Transactions on Communications, 2009, 57, 3732-3742.	4.9	1
33	Coarse optical circuit switching by default, rerouting over circuits for adaptation. Journal of Optical Networking, 2009, 8, 33.	2.5	6
34	Proactive Surge Protection: A Defense Mechanism for Bandwidth-Based Attacks. IEEE/ACM Transactions on Networking, 2009, 17, 1711-1723.	2.6	25
35	Optimal multi-path routing and bandwidth allocation under utility max-min fairness. , 2009, , .		16
36	The Taming of the Shrew: Mitigating Low-Rate TCP-Targeted Attack. , 2009, , .		3

#	Article	IF	Citations
37	Custom Networks-on-Chip Architectures With Multicast Routing. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2009, 17, 342-355.	2.1	23
38	A Layer-Multiplexed 3D On-Chip Network Architecture. IEEE Embedded Systems Letters, 2009, 1, 50-55.	1.3	28
39	A randomized interleaved DRAM architecture for the maintenance of exact statistics counters. Performance Evaluation Review, 2009, 37, 53-54.	0.4	3
40	Design of application-specific 3D Networks-on-Chip architectures. , 2008, , .		28
41	Application-specific Network-on-Chip architecture synthesis based on set partitions and Steiner Trees. , 2008, , .		7
42	BRICK. , 2008, , .		30
43	Near-optimal oblivious routing on three-dimensional mesh networks. , 2008, , .		15
44	DRAM is plenty fast for wirespeed statistics counting. Performance Evaluation Review, 2008, 36, 45-51.	0.4	8
45	Frame-aggregated concurrent matching switch. , 2007, , .		2
46	Fast Buffer Memory with Deterministic Packet Departures. , 0, , .		11