

Nael Mizanur Rahman

List of Publications by Year in descending order

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#	ARTICLE	IF	CITATIONS
1	Chiplet/Interposer Co-Design for Power Delivery Network Optimization in Heterogeneous 2.5-D ICs. IEEE Transactions on Components, Packaging and Manufacturing Technology, 2021, 11, 2148-2157.	2.5	5
2	Processing-In-Memory-Based On-Chip Learning With Spike-Time-Dependent Plasticity in 65-nm CMOS. IEEE Solid-State Circuits Letters, 2020, 3, 278-281.	2.0	9
3	A Flexible Precision Multi-Format In-Memory Vector Matrix Multiplication Engine in 65 nm CMOS With RF Machine Learning Support. IEEE Solid-State Circuits Letters, 2020, 3, 450-453.	2.0	2
4	Architecture, Chip, and Package Codesign Flow for Interposer-Based 2.5-D Chiplet Integration Enabling Heterogeneous IP Reuse. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2020, 28, 2424-2437.	3.1	32
5	Aging Challenges in On-chip Voltage Regulator Design. , 2020, , .		0
6	A Configurable Dual-Mode PRINCE Cipher with Security Aware Pipelining in 65nm for High Throughput Applications. , 2020, , .		1
7	A Fully Synthesized Integrated Buck Regulator with Auto-generated GDS-II in 65nm CMOS Process. , 2020, , .		2
8	An Authentication IC with Visible Light Based Interrogation in 65nm CMOS. , 2020, , .		1